VT86C100A

PCI FAST ETHERNET CONTROLLER

Revision 0.3
September 25, 1998

VIA TECHNOLOGIES, INC.

Copyright Notice:

VT86C100A may only be used to identify a product of VIA Technologies, Inc.

Disclaimer Notice:

Offices:

USA Office:
1045 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301

Taipei Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 218-5452
Fax: (886-2) 218-5453

Online Services:

Web Page: http://www.via.com.tw –or- http://www.viatech.com
FTP Server: ftp://ftp.via.com.tw
BBS: 886-2-2185208

REVISION HISTORY

Document Release	Date	Revision	Initials
Revision 0.1	8/31/97	Initial release	JC
Revision 0.2	7/30/98	Reformat to VIA standard data sheet format, clean up typos, add mech specs	DH
Revision 0.3	9/24/98	Changed terminology to “Magic Key” Fixed register definitions Rx78[4-6], Rx79[3-4], Rx7A[3-4], Rx7B[2] Fixed typos in alphabetical pin list and page formatting Fixed formatting and alignment in timing diagrams	DH

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VT86C100A
PCI FAST ETHERNET CONTROLLER

- **Single Chip Fast Ethernet Controller for PCI Bus**
  - PCI v2.1 compliant with optional delay transaction and sub-vendor, sub-system- ID
  - Provides a direct connection to the PCI bus
  - -- Supports two network ports and 10 / 100 M MII interface
- **High Performance PCI Mastering Architecture**
  - VIA-defined 128 byte memory I/O or register I/O based command and status registers
  - Software oriented chain structure description to minimize hardware complexity
  - On chip bus master DMA with programmable burst length for low CPU utilization
  - Dynamic transmit packet auto queuing for back to back transmission
  - Programmable activity polling intervals for description DMA
  - Programmable DMA arbitration priority to minimize overflow / under flow conditions
  - Early receive and early transmit interrupt for software parallel processing
  - Interrupt controllable by receive/transmit descriptor list to reduce interrupt service time
- **Standard 100-Mbit MII interface**
  - Supports 100Base-TX with CAT5 UTP, STP and fiber cables
  - Supports 100Base-T4 with CAT3, CAT4, CAT 5 UTP, STP
- **10 / 100Mhz Full Duplex and Half Duplex Operation**
- **Separate 2K byte FIFOs for Receive and Transmit Controllers**
  - Both support bursts up to full Ethernet length
  - Programmable receive and transmit FIFO threshold controls to optimize PCI throughput
- **Flexible dynamically loadable EEPROM algorithm**
  - Load after power-up
  - Dynamic auto reload
  - Embedded programming for configuration modification
  - Dynamic direct programming for manufacturing
- **Physical, Broadcast, and Multicast Address Filtering Using Hashing Function**
- **Magic Key and Wake on Address Filtering**
- **External Bootrom Up To 64K bytes With No External Address Latch**
- **Software Controllable Power Down**
- **Single +5V Supply, 0.5um Standard CMOS Technology**
- **128 pin PQFP Package**
- **PCB Reference Designs & Schematics Available**

OVERVIEW

The VT86C100A **PCI Bus Master** 100 M Fast Ethernet controller is a CMOS VLSI chip designed for easy implementation of CSMA/CD IEEE 802.3u 100M local area networks. Significant features include: twisted-pair interface, PCI Plug & Play compatibility, 32 bit bus mastering, powerful buffer management and Early Interrupt Receive/Transmit.

The VT86C100A integrates a complete bus-master-capable PCI bus interface compliant with PCI specification v2.1. The VT86C100A bus interface is completely software configurable but may optionally be configured via hardware jumpers if desired.

The VT86C100A incorporates two independent 2K byte FIFOs for transmit or receive data from the system interface or to the network interface, providing temporary storage of data, freeing the host system from real-time demands on the network. The VT86C100A has enhanced FIFO management logic to handle up to four received data packets before transfer to the system data buffer. This ability reduces packet loss due to PCI bus mastering arbitration latency.

The VT86C100A supports the Media Independent Interface (MII) network interface. The MII interface is an IEEE 802.3 compliant interface that provides a simple and easy interconnection between the MAC layer and PHY device. This interface has the following characteristics:

- Supports both 10M and 100M data rates
- Contains data and synchronous clock
- 4-bit independent receive and transmit data paths
- Uses TTL signal levels compatible with common CMOS interfaces

The VT86C100A supports power down mode. The BIOS or Network OS device driver can configure Register A to diagnostic mode then set the Power-On bit of the diagnostic port to "on." When the VT86C100A is in Power Down mode, all power to the PCI interface is cut off and the chip clock is stopped.

The VT86C100A can store one “Magic Key” (6 byte Ethernet address) as an external trigger event. When the VT86C100A receives a Magic Key address packet, a power management event interrupt will be generated (on the PME# or GPIO1 pins) to the system. This signal can be used to assert the ATX power PS-ON signal (refer to ATX specification v2.01) or generate a motherboard wake up interrupt (using an available input such as the “ring”-input of the motherboard chipset “South Bridge”).

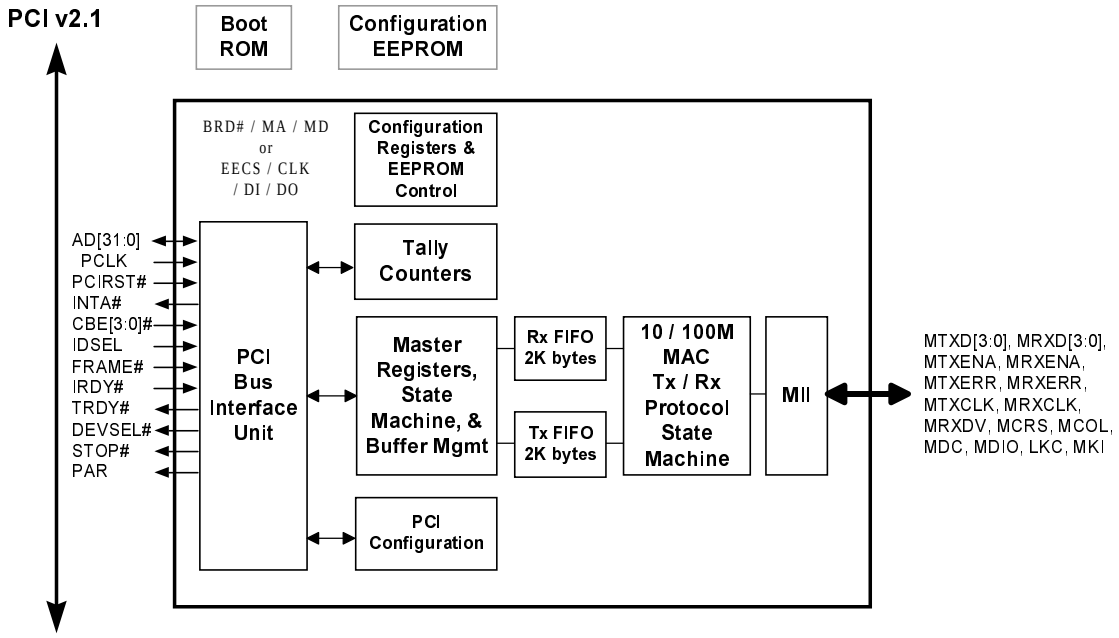


Figure 1. VT86C100A Block Diagram

PINOUTS

Pin Diagram

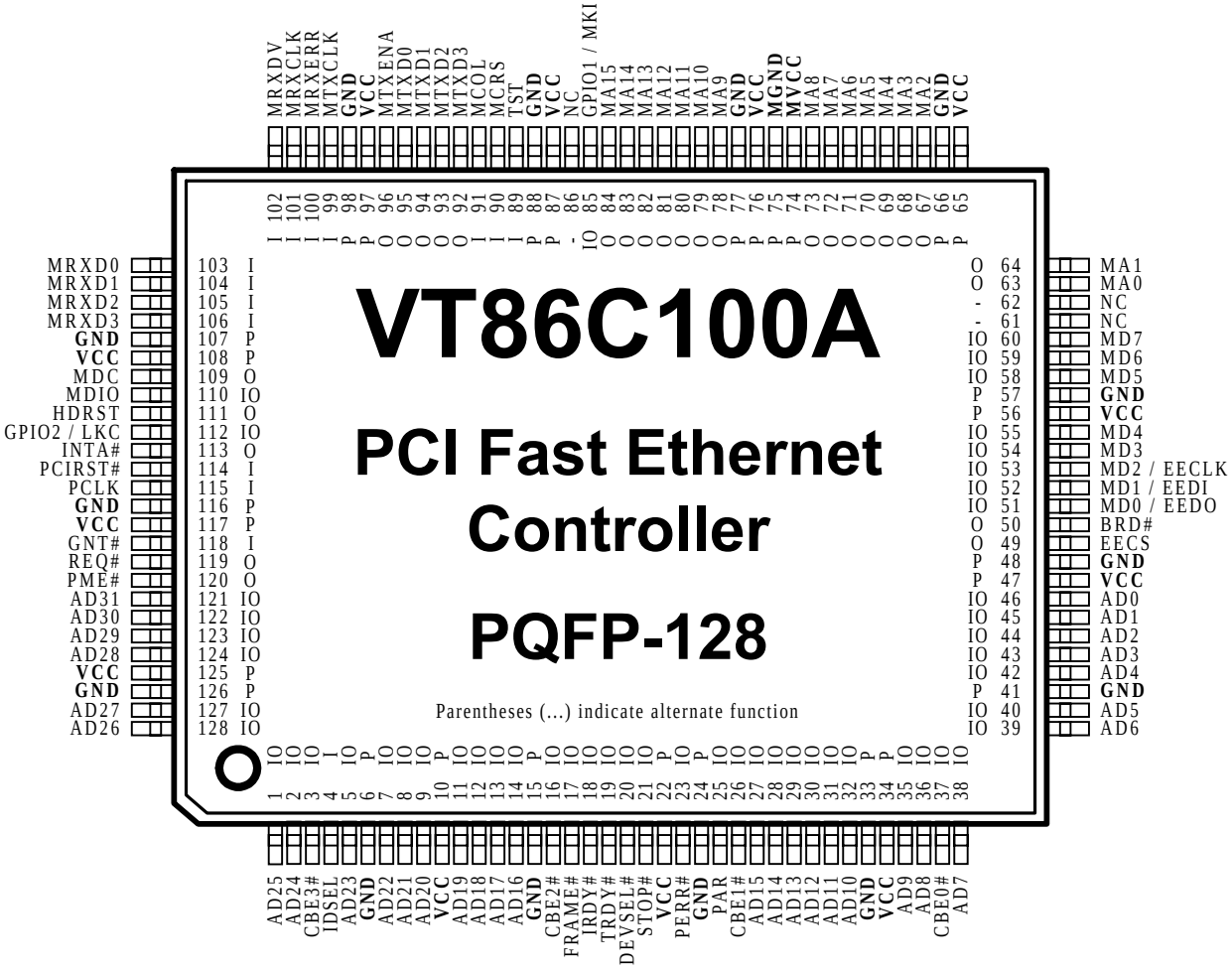


Figure 2. VT86C100A Pin Diagram (Top View)

Pin List

Figure 3. VT86C100A Pin List (Alphabetical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
46	IO	AD00	50	O	BRD#	68	O	MA03	100	I	MRXERR
45	IO	AD01	37	IO	CBE0#	69	O	MA04	99	I	MTXCLK
44	IO	AD02	26	IO	CBE1#	70	O	MA05	95	O	MTXD0
43	IO	AD03	16	IO	CBE2#	71	O	MA06	94	O	MTXD1
42	IO	AD04	3	IO	CBE3#	72	O	MA07	93	O	MTXD2
40	IO	AD05	20	IO	DEVSEL#	73	O	MA08	92	O	MTXD3
39	IO	AD06	49	O	EECS	78	O	MA09	96	O	MTXENA
38	IO	AD07	17	IO	FRAME#	79	O	MA10	**74**	**P**	**MVCC**
36	IO	AD08	**6**	**P**	**GND**	80	O	MA11	61	-	NC
35	IO	AD09	**15**	**P**	**GND**	81	O	MA12	62	-	NC
32	IO	AD10	**24**	**P**	**GND**	82	O	MA13	86	-	NC
31	IO	AD11	**33**	**P**	**GND**	83	O	MA14	25	IO	PAR
30	IO	AD12	**41**	**P**	**GND**	84	O	MA15	114	I	PCIRST#
29	IO	AD13	**48**	**P**	**GND**	91	I	MCOL	115	I	PCLK
28	IO	AD14	**57**	**P**	**GND**	90	I	MCRS	23	IO	PERR#
27	IO	AD15	**66**	**P**	**GND**	51	IO	MD0 / EEDO	120	O	PME#
14	IO	AD16	**77**	**P**	**GND**	52	IO	MD1 / EEDI	119	O	REQ#
13	IO	AD17	**88**	**P**	**GND**	53	IO	MD2 / EECLK	21	IO	STOP#
12	IO	AD18	**98**	**P**	**GND**	54	IO	MD3	19	IO	TRDY#
11	IO	AD19	**107**	**P**	**GND**	55	IO	MD4	89		TST
9	IO	AD20	**116**	**P**	**GND**	58	IO	MD5	**10**	**P**	**VCC**
8	IO	AD21	**126**	**P**	**GND**	59	IO	MD6	**22**	**P**	**VCC**
7	IO	AD22	118	I	GNT#	60	IO	MD7	**34**	**P**	**VCC**
5	IO	AD23	85	IO	GPIO1 / MKI	109	O	MDC	**47**	**P**	**VCC**
2	IO	AD24	112	IO	GPIO2 / LKC	110	IO	MDIO	**56**	**P**	**VCC**
1	IO	AD25	111	O	HDRST	**75**	**P**	**MGND**	**65**	**P**	**VCC**
128	IO	AD26	4	I	IDSEL	101	I	MRXCLK	**76**	**P**	**VCC**
127	IO	AD27	113	O	INTA#	103	I	MRXD0	**87**	**P**	**VCC**
124	IO	AD28	18	IO	IRDY#	104	I	MRXD1	**97**	**P**	**VCC**
123	IO	AD29	63	O	MA00	105	I	MRXD2	**108**	**P**	**VCC**
122	IO	AD30	64	O	MA01	106	I	MRXD3	**117**	**P**	**VCC**
121	IO	AD31	67	O	MA02	102	I	MRXDV	**125**	**P**	**VCC**

Pin Descriptions

Table 1. VT86C100A Pin Descriptions

PCI Bus Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
AD[31:0]	121-124, 127-128, 1-2, 5, 7-9, 11-14, 27-32, 35-36, 38-40, 42-46	IO	**Address / Data Bus.** Address and data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted.
CBE[3:0]#	3, 16, 26, 37	IO	**Command / Byte Enable**. Bus Command/Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, CBE3-0# define the Bus Command. During the data phase, CBE3-0# are used as Byte Enables. The Byte Enables define which physical byte lanes carry meaningful data. CBE0# applies to byte 0 and CBE3# applies to byte 3.
FRAME#	17	IO	**Frame.** Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
DEVSEL#	20	IO	**Device Select.** Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
TRDY#	19	IO	**Target Ready.** Target Ready indicates the target agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a read, TRDY# indicates that valid data is present on AD31-0. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
IRDY#	18	IO	**Initiator Ready.** Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a write, IRDY# indicates that valid data is present on AD31-0. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
REQ#	119	O	**Bus Request.** Asserted by the bus master to indicate to the bus arbiter that it wants to use the bus.
GNT#	118	I	**Bus Grant.** Asserted to indicate to the VT86C100A that access to the bus is granted.
IDSEL	4	O	**ID Select.** Used as a chip select during PCI configuration cycles.
INTA#	113	O	**Interrupt.** An asynchronous signal used to request an interrupt.
PCLK	115	I	**PCI Clock.** Provides timing for all transactions on the PCI bus and is an input pin to every PCI device.
PCIRST#	114	I	**Reset.** When asserted low, the VT86C100A performs an internal hardware reset. PCIRST# may be asynchronous to PCICLK when asserted or deasserted. However, it is recommended that the deassertion is synchronous to guarantee a clean and bounce free edge.
PAR	25	IO	**Parity.** Parity is even across AD31-0 and CBE3-0#. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.
PERR#	23	O	**Parity Error.** Parity error is asserted when a data parity error is detected.
STOP#	21	IO	**Stop.** The VT86C100A drives STOP# to disconnect further transactions.

External Memory Interface and General Purpose I/O			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
EECS	49	O	**EEPROM Chip Select.** Chip select signal for the external EEPROM when an EEPROM is used to provide configuration data and Ethernet Address. A 100K pull-up resistor is provided internally.
EEDO / MD0	51	O / I	**EEPROM Data Out.**
EEDI / MD1	52	I / I	**EEPROM Data In.**
EECLK / MD2	53	O / I	**EEPROM Clock.**
MD[7:0]	60-58, 55-51	I	**BootROM Data.**
MA[15:0]	84-78, 73-67, 64-63	O	**BootROM Address.**
BRD#	50	O	**BootROM Read.**
GPIO1 / MKI	85	IO	**General Purpose I/O 1.** General purpose input / output. Typically used as Magic Key Interrupt.
GPIO2 / LKC	112	IO	**General Purpose I/O 2.** General purpose input / output. Typically used as Link Change Status.

Network Interface			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
MTXD[3-0]	92-95	O	**MII Transmit Data.** Synchronous to the assertion of MTXCLK.
MTXENA	96	O	**MII Transmit Data Enable.** Signals that an MII port transmit operation is active to an external PHY device.
MTXCLK	99	I	**MII Transmit Clock.** Supports a 25 MHz or 2.5 MHz transmit clock supplied by the external PHY device. This clock should always be active.
MRXD[3-0]	106-103	I	**MII Receive Data.** Driven from the external PHY device synchronous with MRXCLK.
MRXDV	102	I	**MII Receive Data Valid.**
MRXERR	100	I	**MII Receive Error.** Asserted when a data decoding error is detected by the external PHY device.
MRXCLK	101	I	**MII Receive Clock.** Supports either 25 MHz or 2.5 MHz clocks. This clock is recovered by the PHY device.
MDC	109	O	**MII Management Data Clock.** Sourced by the VT86C100A MDC bit (MIIR:0) to external PHY devices as a timing reference for the MDIO signal.
MDIO	110	IO	**MII Management Data.** Read from the MDI bit (MIIR:1) or written from the MDO bit (MIIR:2)
MCOL	91	I	**Collision Detect.** From the external PHY device.
MCRS	90	I	**Carrier Sense.** From the external PHY device, asserted when the media is active.
LKC / GPIO2	112	I	**Link Change Status.** From the external PHY device.
MKI / GPIO1	85	O	**Magic Key Intrerrupt.**

Miscellaneous			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
HDRST			**Hardware Reset.**
PME#	120	O	**Power Management Event Interrupt.**
NC	61, 62, 86	-	**No Connection.**
TST	89		**Test.**

Power and Ground			
Signal Name	**Pin No.**	**I/O**	**Signal Description**
GND	6, 15, 24, 33, 41, 48, 57, 66, 77, 88, 98, 107, 116, 126	P	**Ground.**
VCC	10, 22, 34, 47, 56, 65, 76, 87, 97, 108, 117, 125	P	**Power.**
MGND	75	P	**Memory Interface Ground.**
MVCC	74	P	**Memory Interface Power.**

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT86C100A. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 2. VT86C100A Registers

PCI Function 0 Registers – Controller Configuration

Configuration Space Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3043	RO
5-4	Command	0000	**RW**
7-6	Status	0280	**WC**
8	Revision ID	nn	RO
9	Programming Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	02	RO
C	Cache Line Size	00	**RW**
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	-reserved- (Built In Self Test)	00	—
13-10	CSR Memory Map Base Address	0000 0001	**RW**
17-14	CST I/O Map Base Address	0000 0000	**RW**
18-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2C-2F	-reserved- (subsystem ID read)	00	—
33-30	Expansion ROM Base Address	0000 0000	**RW**
34-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	01	RO
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space Controller-Specific Registers

Offset	Heading	Default	Acc
40-4F	-reserved-	00	—
50	Mode 0	00	RW
51	FIFO Test	00	RW
52	Mode 2	00	RW
53	Mode 3	00	RW
54-FF	-reserved-	00	—

Memory-Space Registers

Offset	Heading	Default	Acc
05-00	Par / Key	00 … 00	RW
06	Receive Configuration	00	RW
07	Transmit Configuration	00	RW
08	Command 0	00	RW
09	Command 1	00	RW
0A-0B	-reserved-	—	—
0D-0C	Interrupt Status	0000	RW
0F-0E	Interrupt Mask	0000	RW
17-10	MAR	00 … 00	RW
1B-18	Current Receive Descriptor Addr	0000 0000	RW
1F-1C	Current Transmit Descriptor Addr	0000 0000	RW
2F-20	Current Receive Descriptor	00 … 00	**RO**
3F-30	Next Receive Descriptor	00 … 00	**RO**
4F-40	Current Transmit Descriptor	00 … 00	**RO**
5F-50	Next Transmit Descriptor	00 … 00	**RO**
63-60	Current Receive DMA Pointer	0000 0000	RW
67-64	Current Transmit DMA Pointer	0000 0000	RW
6B-68	Tally Counter Test	0000 0000	RW
6C	Physical Address	00	RW
6D	MII Status	00	RW
6F-6E	BCR	0000	RW
70	MII Command	00	RW
71	MII Address	00	RW
73-72	MII Data	0000	RW
74	EEPROM Status	00	RW
75	Test	00	RW
76	General Purpose I/O	00	RW
77	-reserved-	—	—
78	Configuration A	00	RW
79	Configuration B	00	RW
7A	Configuration C	00	RW
7B	Configuration D	00	RW
7D-7C	Tally Counter MPA	0000	RW
7F-7E	Tally Counter CRC	0000	RW

Register Descriptions

Configuration Registers (Function 0)

There are three sets of software accessible registers: configuration registers, memory space registers, and I/O space registers. The configuration registers are located in the function 0 PCI configuration space. The memory registers are located in system memory space at offsets from the address stored in the CSR Memory Map Base Address Register. The I/O registers are located in system I/O space at offsets from the I/O address stored in the CSR I/O Map Base Address Register.

Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

0-7 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

0-7 Device ID (3043h = VT86C100A Ethernet Controller)

Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Enable .....fixed at 0 (disabled)

8 SERR# Enable .....fixed at 0 (disabled)

7 Wait Cycle Control .....fixed at 0 (disabled)

6 Parity Error Response .....fixed at 0 (disabled)

5 VGA Palette Snoop .....fixed at 0 (disabled)

4 Postable Memory Write Enable fixed at 0 (disabled)

3 Special Cycle Enable .....fixed at 0 (disabled)

2 Bus Master Enable

0 Disable .....default

1 Enable

1 Memory Space Enable

0 Disable .....default

1 Enable Access to Memory Registers

0 I/O Space Enable

0 Disable .....default

1 Enable Access to I/O Registers

Offset 7-6 - Status ..... RWC

15 Detected Parity Error .....always reads 0

14 Signalled System Error .....always reads 0

13 Received Master Abort

0 No Master Abort Generated..... default

1 Master Abort Generated by the VT86C100A Controller. Set by the VT86C100A interface logic if it generates a master abort while acting as a master. This bit may be cleared by software by writing a one to this bit posiition.

12 Received Target Abort

0 No Target Abort Received..... default

1 Target Abort Received by the VT86C100A Controller. Set by the VT86C100A interface logic if it receives a target abort while acting as a master. This bit may be cleared by software by writing a one to this bit posiition.

11 Signalled Target Abort .....always reads 0

10-9 DEVSEL# Timing

00 Fast

01 Medium

10 Slow ..... fixed

11 Reserved

8 Data Parity Error Detected .....always reads 0

7 Fast Back-to-Back Capable .....always reads 1

6 User Definable Features.....always reads 0

5 66 MHz Capable.....always reads 0

4-0 Reserved .....always reads 0

Offset 8 - Revision ID (nnh)..... **RO**

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h)..... **RO**

Offset A - Sub Class Code (00h) ..... **RO**

Offset B - Base Class Code (02h) ..... **RO**

Offset C - Cache Line Size (00h) .....**RW**

7-0 Cache Line Size

Offset D - Latency Timer (00h) .....**RW**

7-4 Latency Timer Count
PCI burst cycles generated by the VT86C100A can last indefinitely as long as PCI GNT# remains active. If GNT# is negated after the burst is initiated, the VT86C100A limits the duration of the burst to the number of PCI Bus clocks specified in this field.

3-0 Reserved ..... always reads 0

Offset E - Header Type (00h) .....**RO**

Offset F – Built In Self Test (00h) .....**RO**

Offset 13-10 – CSR Memory Map Base Address.....**RW**

31-7 Base Address (128-Byte Space)..... default = 0

6-4 Reserved ..... always reads 0

3 Prefetechable..... always reads 0
Reads 0 to indicate that the 86C100A register space is not prefetchable.

2-1 Type ..... always reads 0
Reads 0 to indicate that the 86C100A register space may be located anywhere in the 32-bit address space.

0 Resource Type..... always reads 0
Reads 0 to indicate a request for memory space

Offset 17-14 – CSR I/O Map Base Address .....**RW**

31-12 Base Address (4096-Byte Space)..... default = 0

11-4 Reserved ..... always reads 0

3 Prefetechable..... always reads 0
Reads 0 to indicate that the 86C100A register space is not prefetchable.

2-1 Type ..... always reads 0
Reads 0 to indicate that the 86C100A register space may be located anywhere in the 32-bit address space.

0 Resource Type..... always reads 0
Reads 0 to indicate a request for memory space.

Offset 2D-2C – Sub-Vendor ID ..... **RO**

15-0 Sub-Vendor ID

Offset 2F-2E – Sub-System ID..... **RO**

15-0 Sub-System ID

Offset 33-30 – Expansion ROM Base Address..... **RW**

31-14 Base Address (16KB-Byte Space) .....default = 0

13-4 Reserved .....always reads 0

3 Prefetechable.....always reads 0
Reads 0 to indicate that the expansion ROM space is not prefetchable.

2-1 Type .....always reads 0
Reads 0 to indicate that the expansion ROM space may be located anywhere in the 32-bit address space.

0 Resource Type .....always reads 0
Reads 0 to indicate a request for memory space.

Offset 3C - Interrupt Line (00h).....**RO**

Offset 3D - Interrupt Pin (01h=Drives INTA#)..... **RO**

Controller-Specific Configuration Registers

Offset 50 – Mode 0 .....RW

7-1	**Reserved**	..... always reads 0
0	**xx**	
	0 xx	.....default
	1 xx	
	Description	

Offset 51 – FIFO Test .....RW

Offset 52 – Mode 2 .....RW

Offset 53 – Mode 3 .....RW

Memory-Space Registers

These registers occupy a 128-byte space in system memory (offsets 0-7Fh). This address space begins at the address contained in the VT86C100A Configuration Space "CSR Base Address Register" (Function 0 Configuration Space Offset 10h).

Writes to reserved addresses have undefined results and reads from reserved addresses return indeterminate data. Unless specified otherwise, all register fields default to 0.

Table 3. Memory-Space Register Summary

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	PAR0	R/W	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
01H	PAR1	R/W	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
02H	PAR2	R/W	D23	D22	D21	D20	D19	D18	D17	D16
03H	PAR3	R/W	D31	D30	D29	D28	D27	D26	D25	D24
04H	PAR4	R/W	D39	D38	D37	D36	D35	D34	D33	D32
05H	PAR5	R/W	D47	D46	D45	D44	D43	D42	D41	D40
06H	RCR	R/W	RRFT2	RFT1	RFT0	PROM	AB	AM	AR	SEP
07H	TCR	R/W	RTSF	RTFT1	RTFT0		OFST	LB1	LB0	
08H	CR0	R/W		RDMD	TDMD	TXON	RXON	STOP	STRT	INIT
09H	CR1	R/W	SRST	RDMD1	TDMD1	KEYPAG	DPOLL	FDX	ETEN	EREN
0AH										
0BH										
0CH	ISR0	R/W	CNT	BE	RU	TU	TXE	RXE	PTX	PRX
0DH	ISR1	R/W	KEYI	SRCI	ABTI	NBFI	PRAI	OVFI	ETI	ERI
0EH	IMR0	R/W	CNTM	BEM	RUM	TUM	TXEM	RXEM	PTXM	PRXM
0FH	IMR1	R/W	KEYIM	SRCM	ABTM	NBFM	PRAIM	OVFM	ETM	ERM
10H	MAR0	R/W	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
11H	MAR1	R/W	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
12H	MAR2	R/W	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
13H	MAR3	R/W	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
14H	MAR4	R/W	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
15H	MAR5	R/W	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
16H	MAR6	R/W	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
17H	MAR7	R/W	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56
18H	RDA0	R/W	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
19H	RDA1	R/W	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8
1AH	RDA2	R/W	AB23	AB22	AB21	AB20	AB19	AB18	AB17	AB16
1BH	RDA3	R/W	AB31	AB30	AB29	AB28	AB27	AB26	AB25	AB24
1CH	TDA0	R/W	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
1DH	TDA1	R/W	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8
1EH	TDA2	R/W	AB23	AB22	AB21	AB20	AB19	AB18	AB17	AB16
1FH	TDA3	R/W	AB31	AB30	AB29	AB28	AB27	AB26	AB25	AB24
6CH	MPHY	R/W	MPO1	MPO0		PHYAD4	PHYAD3	PHYAD2	PHYAD1	PHYAD0
6DH	MIISR	R/W	GPIO1POL	LEDPOL	MFDC	PHYOPT	MIIERR	MRERR	LNKFL	SPEED
6EH	BCR0	R/W		REQOPT	CRFT2	CRFT1	CRFT0	DMAL2	DMAL1	DMAL0
6FH	BCR1	R/W			CTSF	CTF1	CTF0	POT2	POT1	POT0
70H	MIICR	R/W	MAUTO	RCMD	WCMD	MDPM	MOUT	MDO	MDI	MDC
71H	MIIAD	R/W		MSRCEN	MDONE	MAD4	MAD3	MAD2	MAD1	MAD0
72H										
73H										
74H	EECSR	R/W	EEPR	EMBP	LOAD	DPM	ECS	ECK	EDI	EDO
75H	TEST	R/W	HBDIS	FCOL	BKOFF	TSTOVF	TSTUDF	TEST2	TEST1	TEST0
76H										
77H										
78H	CFGA	R/W	EELOAD	JUMPER	MMIOEN	MIIOPT	AUTOOPT	MT10ENO	MT10ENO	MT10EOE
79H	CFGB	R/W	QPKTDIS	TPACEN	MRDM	TXARBIT	RXARBIT	MWWAIT	MRWAIT	LATMEN
7AH	CFGC	R/W		BROPT	DLYEN	DTSEL	BTSEL	BPS2	BPS1	BPS0
7BH	CFGD	R/W	GPIOEN	DIAG	MRDLEN	MAGIC	CRADOM	CAP	MBA	BAKOPT
7CH	MPAC0	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
7DH	MPAC1	R/W	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8
7EH	CRCC0	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
7FH	CRCC1	R/W	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8

Note :
The shaded areas denote that those bits are also selective via external configuration jumpers.

All reserved bit must be zero.

Node Address Registers

Memory Offset 5-0 – PAR / KEY .....RW

47-0 Par / Key Data

Receive / Transnit Configuration Registers

Memory Offset 06h – Receive Configuration .....RW

This register reflects NIC receive configuration and is reset by hardware and software reset.

7-5 Receive FIFO Threshold
- 000 Threshold = 64 bytes.....default
- 001 Threshold = 32 bytes
- 010 Threshold = 128 bytes
- 011 Threshold = 256 bytes
- 100 Threshold = 512 bytes
- 101 Threshold = 768 bytes
- 110 Threshold = 1024 bytes
- 111 Receive store and forward

4 Physical Address Packets Accepted
- 0 Physical address must match node address in PAR0-5 .....default
- 1 All packets with physical destination addresses are accepted

3 Broadcast Packets Accepted
- 0 Packets with broadcast destination are rejected .....default
- 1 Packets with broadcast destination address are accepted

2 Multicast Packets Accepted
- 0 Packets with multicast destination are rejected .....default
- 1 Packets with multicast destination address are accepted

1 Small Packets Accepted
- 0 Packets smaller than 64 bytes are rejected .. def
- 1 Packets smaller than 64 bytes are accepted

0 Error Packets Accepted
- 0 Packets with receive errors are rejected ..... def
- 1 Packets with receive errors are accepted

Memory Offset 06h – Transmit Configuration .....RW

This register reflects NIC transmit configuration and is reset by hardware and software reset.

7-5 Transmit FIFO Threshold
- 000 Threshold = 64 bytes .....default
- 001 Threshold = 32 bytes
- 010 Threshold = 128 bytes
- 011 Threshold = 256 bytes
- 100 Threshold = 512 bytes
- 101 Threshold = 768 bytes
- 110 Threshold = 1024 bytes
- 111 Transmit store and forward (wait until entire packet has been received into the FIFO before starting transmit)

4 Reserved .....always reads 0

3 Backoff Priority Selection
- 0 VIA backoff algorithm.....default
- 1 National Semiconductor compatible algorithm

2-1 Transmit Loopback Mode
- 00 Normal.....default
- 01 Internal loopback
- 10 ENDEC 10BaseT loopback or MII loopback
- 11 223 or other loopback

0 Reserved .....always reads 0

Command / Status Registers

Memory Offset 08h – Command 0.....RW

This register is used to select register pages, enable or disable remote DMA operation, and issue commands

7 Initialize Start
- 0 Normal operation .....default
- 1 Initialize bus master logic

6 Receive Poll Demand
- 0 Disable .....default
- 1 Enable

5 Transmit Poll Demand
- 0 Disable .....default
- 1 Enable

4 Transmit State
- 0 Not in transmit state .....default
- 1 In transmit state (if start bit-1 set)

3 Receive State
- 0 Not in receive state.....default
- 1 In receive state (if start bit-1 set

2 Stopped
- 0 Command procesing is in process .....default
- 1 No command processing is in progress

1 Start
- 0 No command entered.....default
- 1 Start processing a command

0 Reserved ..... always reads 0

Memory Offset 09h – Command 1 .....RW

This register is used to select register pages, enable or disable remote DMA operation, and issue commands

7 Error
- 0 No error
- 1 System Error or Receive Buffer Overflow...def

This bit is cleared by the Start command (CR0 bit-1)

6-4 Reserved .....always reads 0

3 Transmit Auto Polling
- 0 Enable .....default
- 1 Disable

2 Full Duplex Mode
- 0 Set Mac to Half Duplex .....default
- 1 Set MAC to Full Duplex 10 / 100BaseT mode

1 Early Transmit Mode
- 0 Disable .....default
- 1 Enable

0 Early Receive Mode
- 0 Disable .....default
- 1 Enable

Interrupt Status / Mask Registers

Memory Offset 0D-0Ch – Interrupt Status.....RWC

This register reflects NIC status. The host reads it to determine the cause of the interrupt. Individual bits are cleared by writing a one to the corresponding bit. This register must be cleared after power-up.

- **15 Magic Key Packet Received**
- **14 Port Status Changed**
- **13 Transmit Abort**
  Set by excessive collisions
- **12 Receive Buffer Full**
- **11 FIFO Overflow**
  Next packet race with current packet
- **10 Receive FIFO Overflow**
- **9 Transmit Descriptor Underflow**
- **8 Received Packet Has Filled the First Data Buffer**
- **7 CRC Error / Packet Race Tally Counter Overflow**
- **6 PCI Bus Error**
- **5 Receive Buffer Unavailable**
- **4 Transmit Buffer Underflow**
- **3 Transmit Error**
  Set when packet transmission aborted due to excessive collisions
- **2 Receive Error**
  Set by one or more of the following errors: CRC error, Frame Alignment error, or Missed Packet
- **1 Packet Transmitted with No Errors**
- **0 Packet Received with No Errors**

Memory Offset 0F-0Eh – Interrupt Mask..... RWC

All bits in this register correspond to the bits in the Interrupt Status register. Setting individual bits will enable the corresponding interrupt. This register defaults to all zeros on power up.

MII Port Control and Status Registers

Memory Offset 6Ch – MII Configuration.....RW

7-6 MII Management Port Polling Timer Interval
- 00 1024 MDC Clock Cycles
- 01 512 MDC Clock Cycles
- 10 128 MDC Clock Cycles
- 11 64 MDC Clock Cycles

5 Reserved ..... always reads 0

4-0 External PHY Device Address..... default = 00001b
These bits can be loaded from EEPROM during power-up, auto-rreloaded from EEPROM, or can be programmed by software.

Memory Offset 6Dh – MII Status .....RW

7 GPIO1 Output Polarity
- 0 Active low
- 1 Active high

6 Reserved ..... always reads 0

5 Fast MDC Autopolling
- 0 Normal speed
- 1 MDC 4x speed during AutoPolling

4 Fixed PHY Address
- 0 Programmable PHY Address
- 1 Use default PHY address of 00001b

3 PHY Device Receive Error.....RWC
Set if MRXERR asserted

2 MII Management Port Read Error.....RWC

1 Link Fail

0 Network Speed
- 0 100 MHz
- 1 10 MHz

Memory Offset 70h – MII Interface Control .....RW

7 MII Management Port AutoPolling
- 0 Disable.....default
- 1 Enable

6 PHY Status Read
- 0 Read Complete.....default
- 1 Initiate Read (results stored in offset 72h)

5 PHY Program
- 0 Programming Complete .....default
- 1 Initiate PHY Programming

4 Direct PHY Programming Mode
- 0 Disable (bits 0-3 are ignored) .....default
- 1 Enable (bits 5 and 6 are ignored)

3 MDIO Output Enable . (Direct Programming Mode)

2 MDIO Output Level.... (Direct Programming Mode)

1 MDIO Input Status..... (Direct Programming Mode)

0 MDC Output Level..... (Direct Programming Mode)

Memory Offset 71h – MII CSR Offset Address .....RW

7 Reserved .....always reads 0

6 MSRCEN???

5 MDONE???

4-0 MII Management Port Address ....default = 00001b

EEPROM Configuration & Status Registers

Memory Offset 74h – EEPROM Config / Status.....RW

- **7 EEPROM Programming Status**
- **6 EEPROM Embedded Program Enable**
  This bit will be cleared when programming is complete
- **5 Dynamically Reload EEPROM Content**
  PAR5-0 will be updated
- **4 Direct Program EEPROM**
- **3 EEPROM Interface Chip Select Status**
- **2 EEPROM Interface Clock Status**
- **1 EEPROM Interface Data In Status**
- **0 EEPROM Interface Data Out Status**

Configuration Registers

Memory Offset 78 – Configuration A.....RW

7 EEPROM Embedded and Direct Programming
- 0 Disable .....default
- 1 Enable

6 PHY Mode Indicator from External PHY Configuration Signal
.....Loaded from GPIO2 at Reset
- 0 PHY Auto Mode .....default
- 1 PHY Force Mode

5-4 Reserved ..... always reads 0

3 Receive Event Auto Transmit Descriptor Polling
- 0 Disable .....default
- 1 Enable

2 GPIO2 Input Status .....RO
- 0 Low .....default
- 1 High

1 GPIO2 Output Level
- 0 Low .....default
- 1 High

0 GPIO2 Output..... Loaded from MD3 at Reset
- 0 Disable .....default
- 1 Enable

Memory Offset 79 – Configuration B .....RW

7 Transmit Frame Queueing
- 0 Enable .....default
- 1 Disable

6 Transmit Descriptor Pacing Algorithm
- 0 Disable .....default
- 1 Enable

5 Memory Read Multiple
- 0 Not capable .....default
- 1 Capable

4 Transmit Arbitration
- 0 Transmit FIFO DMA continuous.....default
- 1 Transmit FIFO DMA will be interleaved with receive FIFO DMA after 32 double words of the transaction

3 Receive Arbitration
- 0 Receive FIFO DMA continuous .....default
- 1 Receive FIFO DMA will be interleaved with transmit FIFO DMA after 32 double words of the transaction

2 Master Write Insert One Wait State 2-2-2-2
- 0 No .....default
- 1 Yes

1 Master Read Insert One Wait State 2-2-2-2
- 0 No .....default
- 1 Yes

0 Latency Timer
- 0 Disable .....default
- 1 Enable

Memory Offset 7A – Configuration C .....RW

7 Reserved ..... always reads 0

6 BootROM Upper Address Outputs
- 0 Normal BootROM address outputs .....default
- 1 Set BootROM address outputs above the BootROM size selected to logic 1 for small size BootROMs.

5 Delay Transaction While Memory Read BootROM
- 0 Disable .....default
- 1 Enable

4 Reserved ..... always reads 0

3 BootROM Timing Select
- 0 High Speed EPROM .....default
- 1 Low Speed EPROM

2-0 BootROM Size Select
- 000 No Boot ROM.....default
- 001 8KB
- 010 16KB
- 011 32KB
- 1xx 64KB

Memory Offset 7B – Configuration D..... RW

7 GPIO2 Input Status Change Monitor
- 0 Disable ..... default
- 1 Enable

6 Diagnostic Mode
- 0 Disable ..... default
- 1 Enable

5 PCI Memory Read Line Capable
- 0 Not capable ..... default
- 1 Capable

4 Magic Key
- 0 Disable ..... default
- 1 Enable

3 Random Backoff Algorithm
- 0 Disable ..... default
- 1 Enable

2 Capture Effect Backoff Algorithm
- 0 Disable ..... default
- 1 Enable

1 Modify Backoff Algorithm
- 0 Disable ..... default
- 1 Enable

0 Backoff Algorithm Optional
- 0 Disable ..... default
- 1 Enable

FUNCTIONAL DESCRIPTIONS

EEPROM Interface and Programming

VT86C100A uses an external 93C46 serial EEPROM to store configuration data and Ethernet address.

EEPROM Contents

	D15	D0
3FH	Reserved for 93C46	Reserved for 93C46
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
10H	.	.
0FH	73H	73H
0EH	CFG_D	CFG_C
0DH	CFG_B	CFG_A
0CH	BCR1	BCR0
0BH	MAX_LAT	MIN_GNT
0AH	Reserved	Reserved
09H	KEY5	KEY5
08H	KEY3	KEY2
07H	KEY1	KEY0
06H	Reserved	Reserved
05H	SUBVID1	SUBVID0
04H	SUBSID1	SUBSID0
03H	Reserved	MII_PHYAD
02H	Ethernet Address 5	Ethernet Address 4
01H	Ethernet Address 3	Ethernet Address 2
00H	Ethernet Address 1	Ethernet Address 0

Note 1. The word on location 03H is optional to user's application requirement.
Note 2. Programming 73H into the upper address is required to protect the Ethernet address from being destroyed accidentally
Note 3. The word on location 04H, 05H is sub-System ID, sub-Vendor ID in PCI specification 2.1.

Direct EEPROM Programming

The VT86C100A features an easy way to program external EEPROM in-situ. When RESET is active and if the upper byte of 0FH in the EEPROM is not 73H, the EEPR bit will not be set to indicate that the current EEPROM has not been programmed. This will allow the VT86C100A to enter Direct Programming mode if EELOAD is also set. In this mode the user can directly control the EEPROM interface signals by writing to the ECSR Port and the value on the EECS, ESK and EDI bits will be driven onto the EECS, EECLK (MD2), and EEDI (MD1) outputs respectively. These outputs will be latched so the user can generate a clock on EECLK by repetitively writing 1 then 0 to the appropriate bit. This can be used to generate the EEPROM signals per the 93C46 data sheet.

To read EEPROM data, users have to generate EEPROM interface signals into EECS, EEDI and EECLK as described above and read the data from the EEDO (MD0) input. Reading the Data Transfer Port during programming will not affect latched data on the EECS, EECLK, and EEDI outputs. When the EEPROM has been programmed and verified (remember to program the upper byte of 0EH & 0FH with 73H), the user must give the VT86C100A a power-on reset to return to normal operation and to read in the new data.

Direct Programming mode is mainly used for production to program every bit of the EEPROM. Once the upper byte of 0EH has been programmed with 073H and a power-on reset has been performed, there is no way to change the contents of the EEPROM except for Configuration Registers A, B, and C, which will be discussed in the following paragraph. For more information, refer to EECSR.

Embedded EEPROM Programming

If the upper byte of 0FH of the EEPROM has been programmed to 073H when the VT86C100A is loading EEPROM data during power-on reset, the EEPR bit of the Signature Register will be set to prohibit Direct Programming mode. However, the user can still program configuration registers A, B, and C using the Embedded Programming mode by following the routine specified in the pseudo code below. This operation will work regardless of the value of EECONFIG. The setting of the EELOAD bit of Configuration Register B starts the EEPROM write process. Care should be taken not to accidentally modify the POL and GDLNK bits because these two bits return values independently of the setting. This programming process is ended when the EELOAD bit goes to zero.

```
EEPROM_EMB_PROG ( )
{    // defined constant: CONFIG_B,  EELOAD
     // declared register: value, config_for_A, config_for_B, config_for_C
     // declared function: DISABLE_INTERRUPTS, ENABLE_INTERRUPTS, READ, WRITE, WAIT
     DISABLE_INTERRUPTS ( );
     value = READ (CONFIG_B);
     value = value | EELOAD;
     WRITE (CONFIG_B, value);
     READ (CONFIG_B);
     WRITE (CONFIG_B, config_for_A);
     WRITE (CONFIG_B, config_for_B);
     WRITE (CONFIG_B, config_for_C);
     while (value || EELOAD)
     {
          value = READ (CONFIG_B);
          WAIT ( );
     }
     ENABLE_INTERRUPTS ( );
}
```

Buffer Management & Host Communication

The VT86C100A provides a simple and effective buffer management and host communication method through PCI Bus mastering. There are two descriptor lists, one for receive and one for transmit. The bases of these two lists point to the CRDA (18h) and CTDA (1ch) registers.

The descriptor lists reside in the host physical memory address space on **double word boundaries**. Each descriptor list points to a single databuffer, but a data buffer consists of either an entire frame or part of a frame. Data chaining can be enabled or disabled by the DES1 C bit. Data buffers also reside in host physical memory on double word boundaries.

The device driver can program the last descriptor's next link to point to the first descriptor address to create a ring buffer structure.

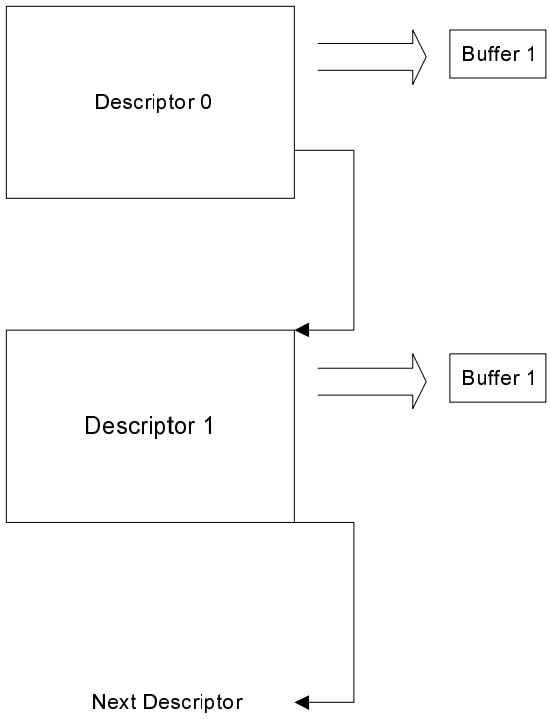


Figure 4 - VT86C100A Buffer Management - Chain Buffer Structure

Descriptor Ring and Chain Structure

Receive Descriptors

Figure 5 shows the receive descriptor format.

The descriptor provides a data buffer address, a byte-count, and a next descriptor address. The chain bit allows data storage to span multiple data buffers and is compatible with various types of memory management schemes.

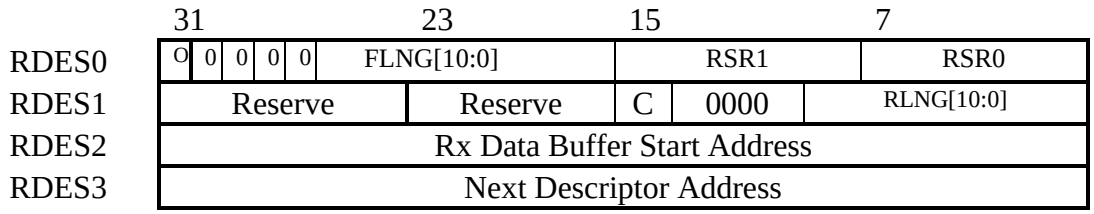


Figure 5 - Receive Descriptor Format

Receive Descriptor 0 (RDES0)

RDES0 contain the received frame status, the frame length and the descriptor ownership information.

Bit		Symbol	Description
31		OWN	**Owner:** This bit is controlled by the driver, 1 indicates that this descriptor is owned by the VT86C100A controller, 0 means this descriptor is free for use. The driver must clear this bit when initialized.
30-27		0000	**Extend Frame Length:** Extend byte count for abnormal size Ethernet frame
26-16		FLNG	**Frame Length:** Received frame length
15-8			
	15	RXOK	**Received OK:** Good packet received from the network
	13	MAR	**Multicast Address Received:** Multicast address packet received
	12	BAR	**Boardcast Address Received:** Broadcast address packet received
	11	PHY	**Physical Address Received:** Physical address received
	10	CHN	**Chain:** means of chain buffer,
	9	STP	**Start of Packet :** In descriptor ring structure, STP=EDP=1 single buffer descriptor, or chained buffer structure as follows: STP EDP Description 1 1 Single buffer descriptor 1 0 First buffer descriptor, further buffer chained 0 1 Chained buffer packet end 0 0 X
	8	EDP	**End of Packet:** End of Packet buffer
7-0		RSR0	**Receive Status Register 0:**
	7	BUFF	**Buffer Error:** Receive Buffer Error
	6	SERR	**System bus error:**
	5	RUNT	**Runt Packet Received:**
	4	LONG	**Long Packet Received:**
	3	FOV	**FIFO Overflow:**
	2	FAE	**Frame Align Error:**
	1	CRC	**CRC Error:** Received frame CRC checksum error
	0	RERR	**Receive Error:** This bit is set by a CRC error, frame alignment error, FIFO overflow, or System bus error.

Receive Descriptor 1 (RDES1)

RDES1 contains the interrupt control enable, the chained frame identical and the receive buffer fragment size information.

Bit	Symbol	Description
31-24	Reserve	
23	IC	**Interrupt Control:** This bit provides support for interrupt PACEing , 1 indicates that the VT86C100A which received this descriptor will generate the interrupt.
23-16	Reserve	
15	C	**Chain:** Chain buffer , 1 indicates that there are chained buffers in the next descriptor
14-11	0000	**Extend Fragment of Frame Length:** Must be zero
10-0	RLEN	**Rx buffer Size:** Receive buffer size for this descriptor, the total byte count of the whole frame will be stored in the last descriptor.

Transmit Descriptors

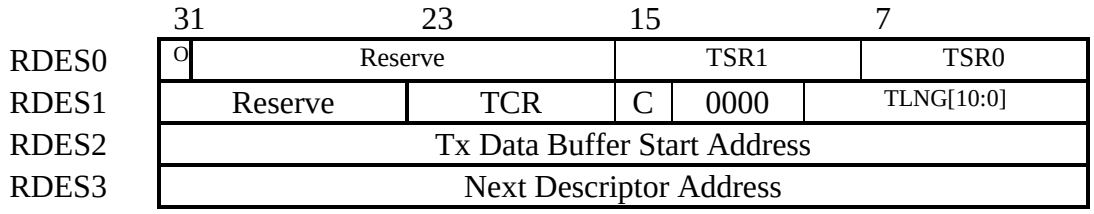


Figure 6 - Transmit Descriptor Format

Transmit Descriptor 0 (TDES0)

TDES0 contains the received frame status, the frame length, and the descriptor ownership information.

Bit	Symbol	Description
31	OWN	**Owner:** This bit is controlled by the driver, 1 indicates that this descriptor is owned by the VT86C100A controller, 0 means this descriptor is free for use. The driver must clear this bit when initialized.
30-24	Reserved	
23-16	TCR	**Transmit Configuration Register**
15-8	TSR1	**Transmit Status Register 1**
15	TXOK	**Transmit OK:** This bit is set to 1 for any transnission error - internal FIFO under-flow - excessive collision (ABT) - late collision (OWC) - carrier sense lost (CRS)
14	JAB	**Jabber:** Jabber condition occurred. Writing to this bit has no effect.
13	SERR	**System Error:** Master abort, target abort, or parity error.
12	Reserve	
11	Reserve	
10	CRS	**Carrier Sense Lost:** Carrier lost during the transmission of a packet.
9	OWC	**Late Collisions:** Late collision occurred.
8	ABT	**Transmit Abort:** Transmit abort due to excessive collisions
7-0	TSR0	**Transmit Status Register 0**
7	CDH	**CD Heartbeat :** This bit is effective in 10Base-T mode only. When set, this bit indicates a heartbeat collision check failure.
6-3	NCR[3:0]	**Collision Retry Count:** This 4-bit counter indicates the number of collisions that occurred
2	Reserved	Reserved
1	UDF	**FIFO Underflow:** This bit set indicates that the transmitter aborted because the transmit FIFO encountered an empty condition while transmitting a frame.
0	DFR	**Deferred:** When set, indicates that the VT86C100A had to defer while ready to transmit a frame because carrier was asserted.

Transmit Descriptor 1 (TDES1)

TDES1 contains the transmit status, the frame length and the descriptor ownership information.

Bit		Symbol	Description
31-24		Reserve	
23-16		TCR	**Transmit Configuration Register**
	23	IC	**Interrupt Control:** This bit supports interrupt PACEing , setting this bit to 1 means the VT86C100A that received this descriptor will generate the interrupt.
	22	EDP	**End of Packet:** End of Packet buffer
	21	STP	**Start of Packet:** In the descriptor ring structure, STP=EDP=1 indicates single buffer descriptor. These bits can also define a chained buffer structure as follows: STP EDP Description 1 1 Single buffer descriptor 1 0 First buffer descriptor, further buffer chained 0 1 Chained buffer packet end 0 0 Reserved
	20 - 17	Reserved	Reserved
	16	CRC	**CRC Disable:** The VT86C100A transmitter will disable CRC generation when this bit is set
15		C	**Chain:** Chain buffer
14-11		0000	**Extend Fragment of Frame Length**: Must be zero.
10-0		TLNG	**Transmit Buffer Size:** Frame buffer fragment size

Buffer Structure and Interrupt Control

A data buffer consists of an entire frame or part of a frame, but it cannot exceed a single Ethernet frame size. Buffers contain only data; All buffer status is maintained in the descriptor. Data chaining can be enabled or disabled by the Chain bit in DES1[15]. Iinterrupt control can also be enabled or disabled by DES1[23].

Multiple Chained Buffer Structure

The VT86C100A can support multiple chain buffers for direct mapping to the OS data buffer. The VT86C100A bus mastering module will directly move the data from the network controller to the OS data buffer or directly transmit the data in OS buffer to the network controller (i.e., it is not necessary to move the data to a temporary data buffer). The data buffer must be double word aligned.

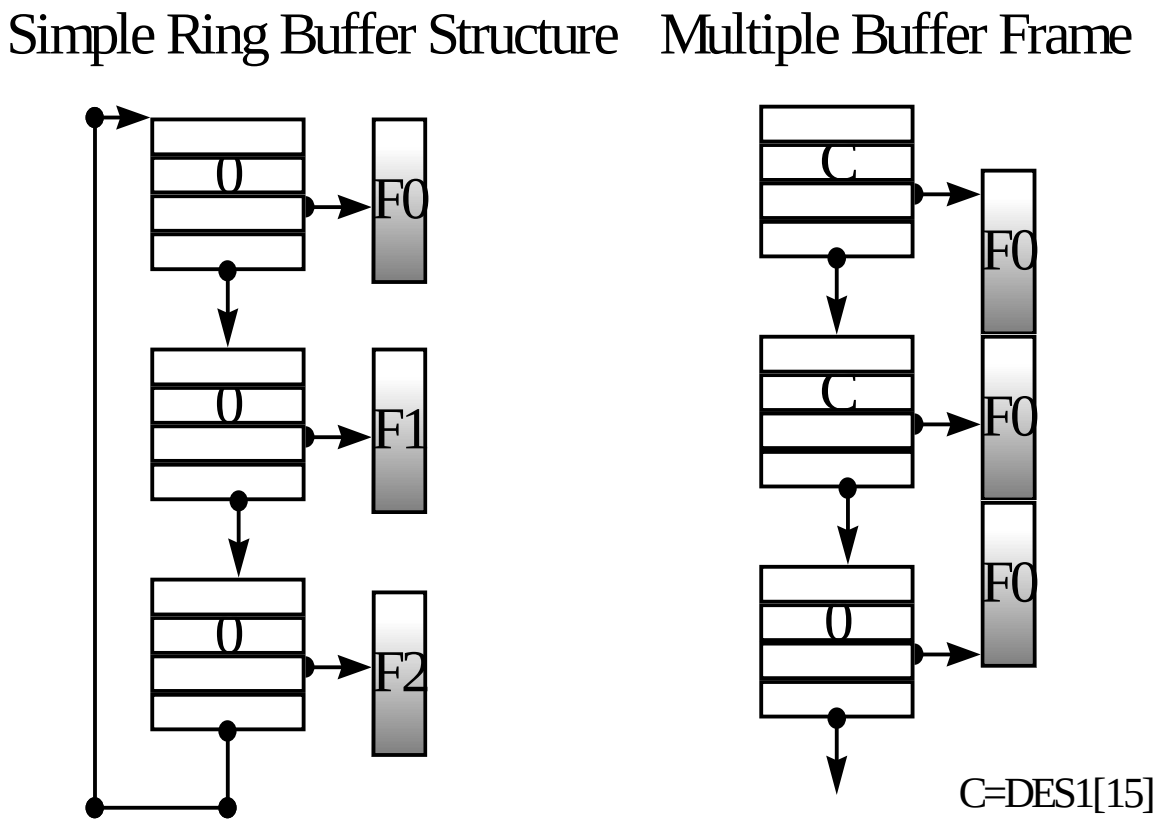


Figure 7 - Ring Buffer and Multiple Buffer Structure

Interrupt Control

The VT86C100A can control the receive and transmit descriptors to determine what interrupts have occured. If the IC bit (DES1[23]) is set to 1, receive or transmit interrupts will be generated independently of whether the frame has been completely received or transmitted. This feature enables the OS to pre-fetch the frame header thus saving interrupt service overload.

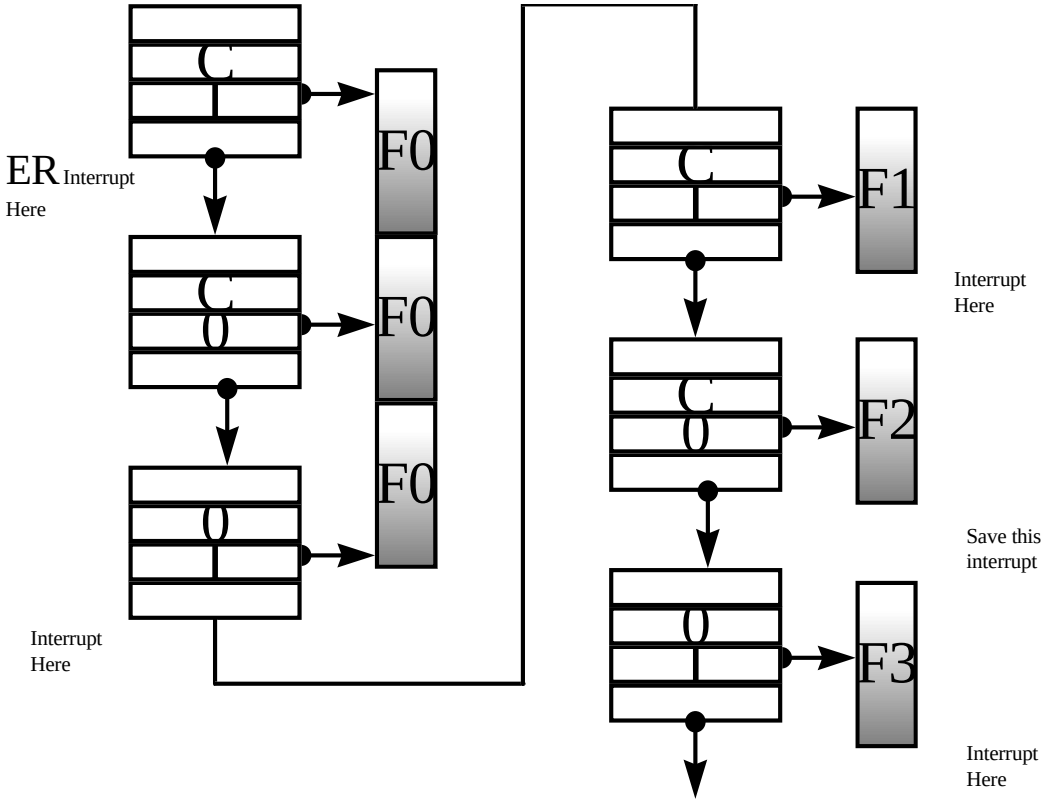
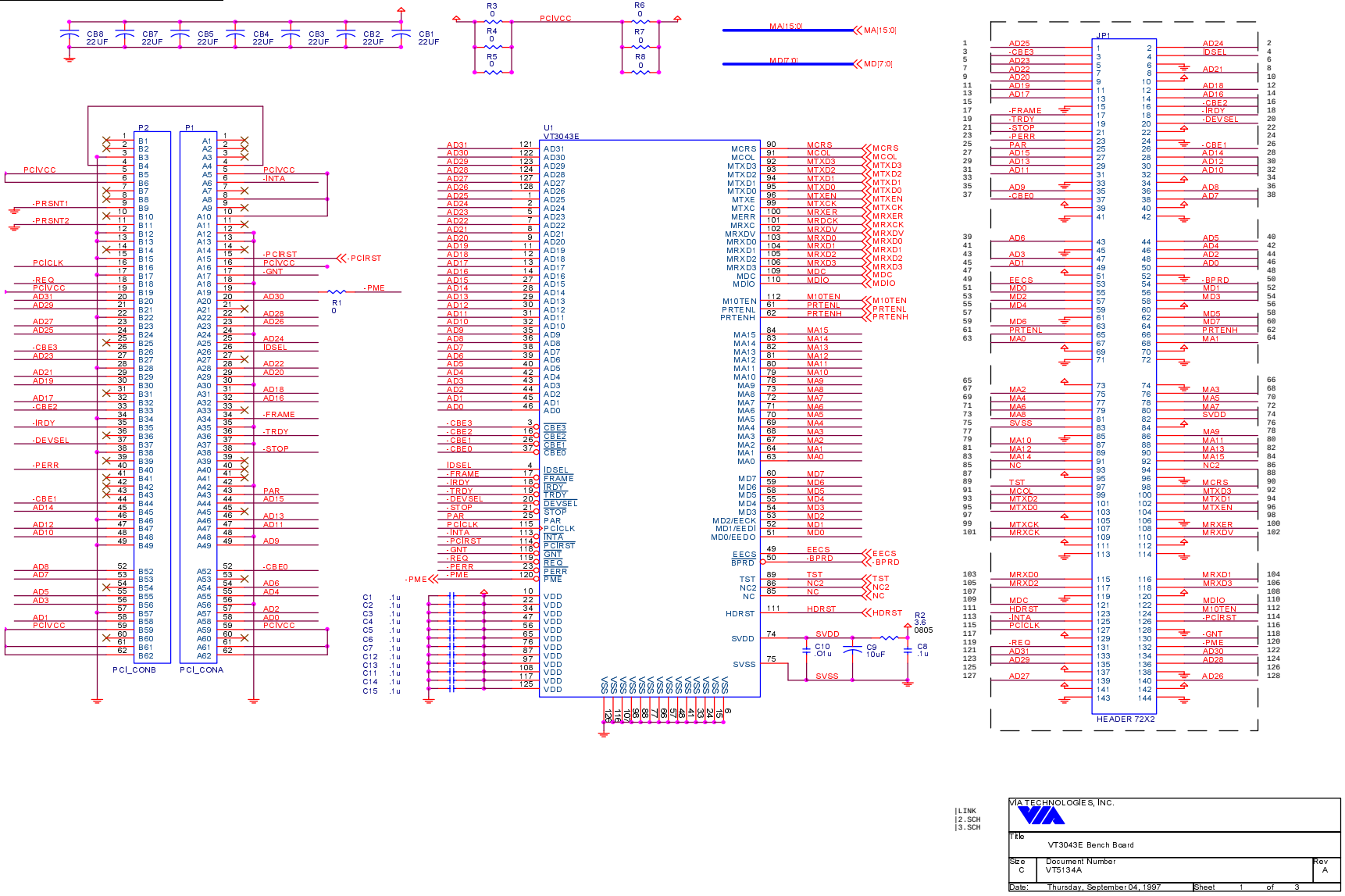


Figure 8 – VT86C100A Interrupt Control

APPLICATION SCHEMATICS

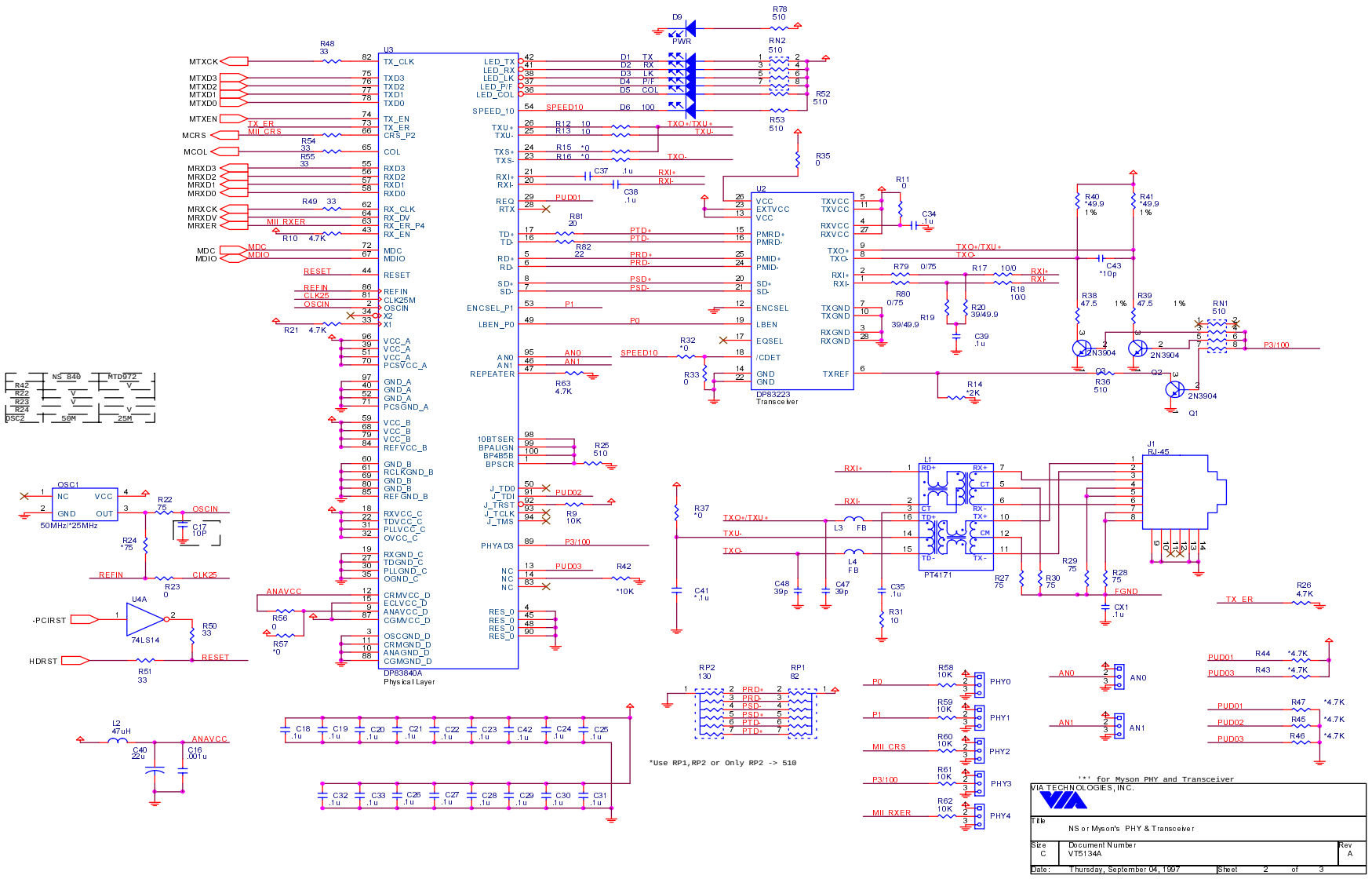
VT3043E Bench Test Board

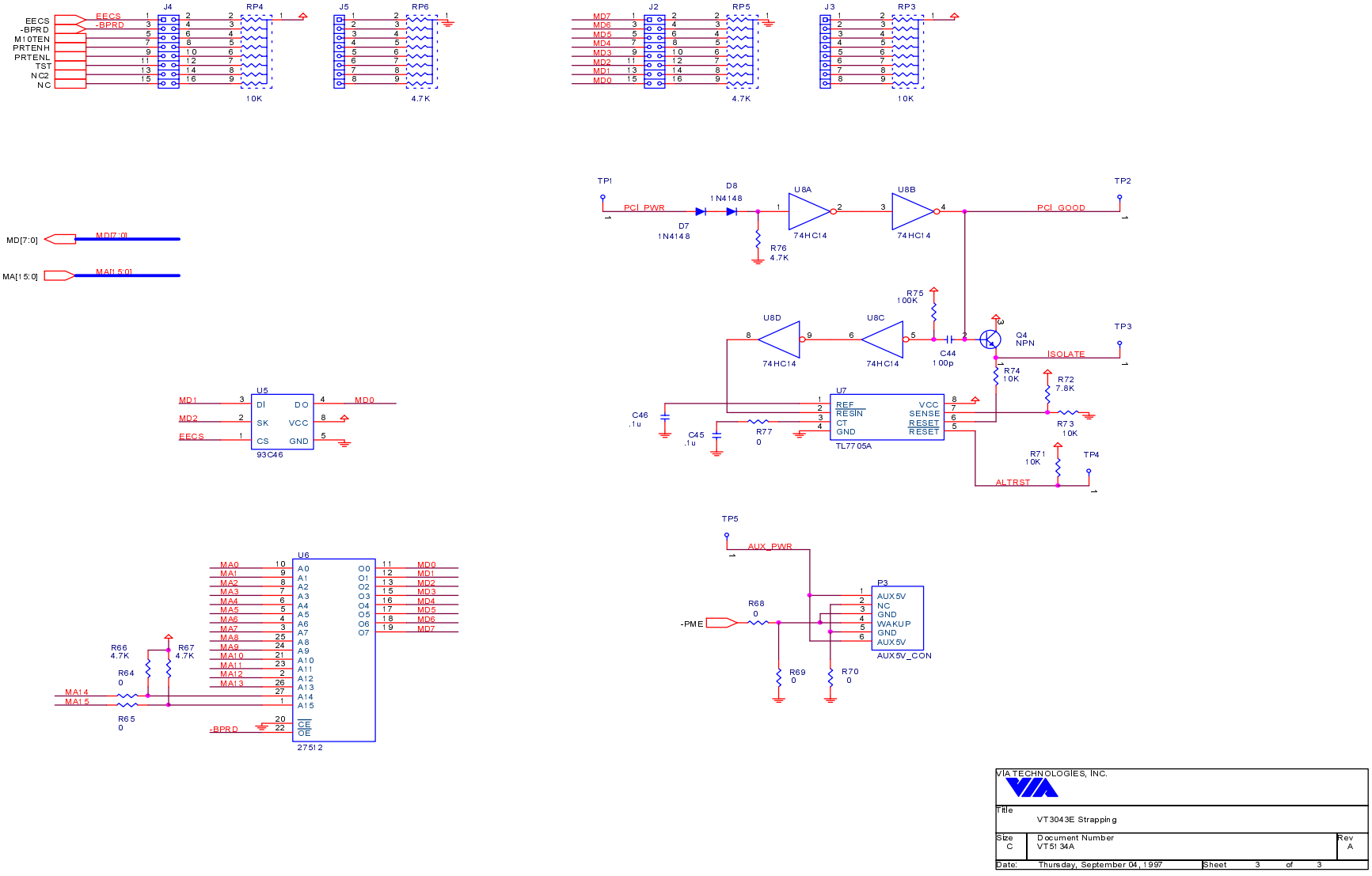


LINK	
2.SCH	
3.SCH	

VIA TECHNOLOGIES, INC.

Title: VT3043E Bench Board		
Size: C	Document Number: VT5134A	Rev: A
Date: Thursday, September 04, 1997	Sheet 1 of 3	


U3
DP83840A
Physical Layer
U2
DP83223
Transceiver
U4A
74LS14
OSC1
50MHz/*25MHz
L1
PT4171
J1
RJ-45
Q1
2N3904
Q2
2N3904
Q3
2N3904
*Use RP1,RP2 or Only RP2 -> 510
'*' for Myson PHY and Transceiver
VIA TECHNOLOGIES, INC.
Title
NS or Myson's PHY & Transceiver
Size C
Document Number VT5134A
Rev A
Date: Thursday, September 04, 1997
Sheet 2 of 3


EECS
-BPRD
M10TEN
PRTENH
PRTENL
TST
NC2
NC
J4
RP4
10K
J5
RP6
4.7K
MD7
MD6
MD5
MD4
MD3
MD2
MD1
MD0
J2
RP5
4.7K
J3
RP3
10K
MD[7:0]
MA[15:0]
TP1
PCI_PWR
D8
1N4148
D7
1N4148
R76
4.7K
U8A
74HC14
U8B
74HC14
TP2
PCI_GOOD
R75
100K
U8D
74HC14
U8C
74HC14
C44
100p
Q4
NPN
TP3
ISOLATE
R74
10K
R72
7.8K
R73
10K
U7
TL7705A
REF
RESIN
CT
GND
VCC
SENSE
RESET
RESET
C46
.1u
C45
.1u
R77
0
R71
10K
TP4
ALTRST
U5
93C46
DI
DO
SK
VCC
CS
GND
MD1
MD2
EECS
MD0
U6
27512
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
MA14
MA15
-BPRD
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
R66
4.7K
R67
4.7K
R64
0
R65
0
TP5
AUX_PWR
P3
AUX5V_CON
AUX5V
NC
GND
WAKUP
GND
AUX5V
-PME
R68
0
R69
0
R70
0
VIA TECHNOLOGIES, INC.
Title
VT3043E Strapping
Size
C
Document Number
VT5134A
Rev
A
Date: Thursday, September 04, 1997
Sheet 3 of 3

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage	4.5	5.5	Volts
Input Voltage	-0.5	V_{CC} + 0.5	Volts
Output Voltage	-0.5	V_{CC} + 0.5	Volts
Storage Temperature	-65	150	^{O}C
Ambient Operating Temperature	0	70	^{O}C
ESD Rating	-	2500	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

TA-0-70^{O}C, V_{CC}=5.0V+/-5%, GND=0V

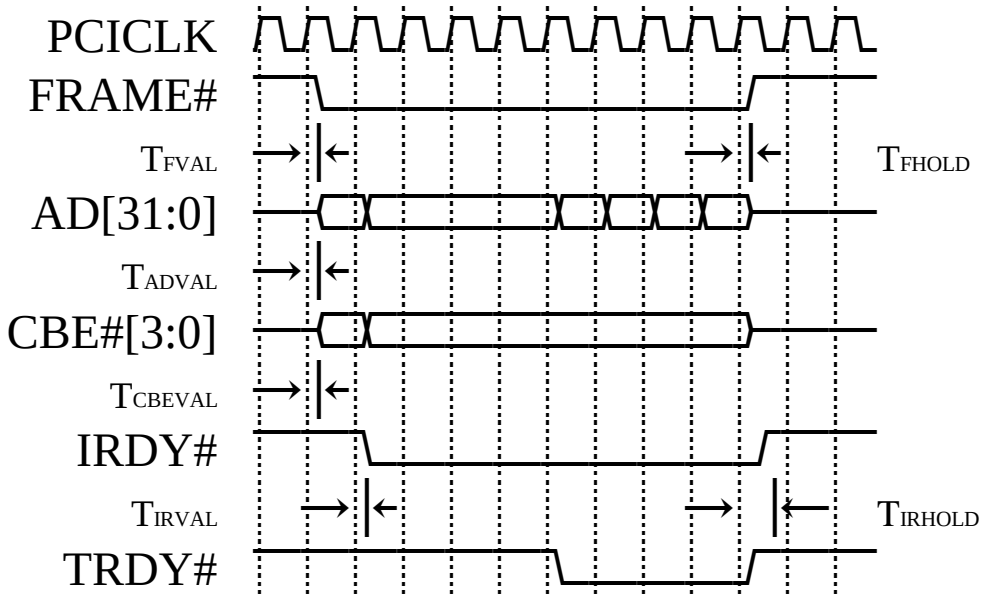
Symbol	Parameter	Min	Max	Unit	Condition
I_{CC}	Supply Current – Average Active		100	mA	X1=25MHz, Vin switching
I_{CCIDLE}	Supply Current – Average Idle		80	mA	X1=25MHz, Vin=Vcc or Gnd
I_{CCLP}	Supply Current – Low Power Mode		35	mA	X1 undriven, Vin = Vcc or Undriven
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
I_{IL}	Input leakage current	-1.0	+1.0	uA	Gnd < V_{IN} < V_{CC}
V_{OL}	Output Low Voltage – High Drive Outputs	-	0.5	V	I_{OL} = 20 uA
V_{OH}	Output High Voltage – High Drive Outputs	2.4	-	V	I_{OH} = -20 uA
V_{OL}	Output Low Voltage – MOS Outputs	-	0.1	V	I_{OL} = 20 uA
V_{OH}	Output High Voltage – MOS Outputs		V_{CC}-0.1	V	I_{OH} = -20 uA
V_{OL}	Output Low Voltage – O.C. Outputs	-	0.5	V	I_{OL} = 24 mA
I_{OZ}	Tristate Leakage Current	-10	+10	uA	Gnd < V_{OUT} < V_{CC}

Note 1: These parameters are not guaranteed by production testing. All electrical specifications are based on IEEE 802.3 requirements and internal design considerations.

AC Characteristics

Bus Arbitration and Mastering Timing

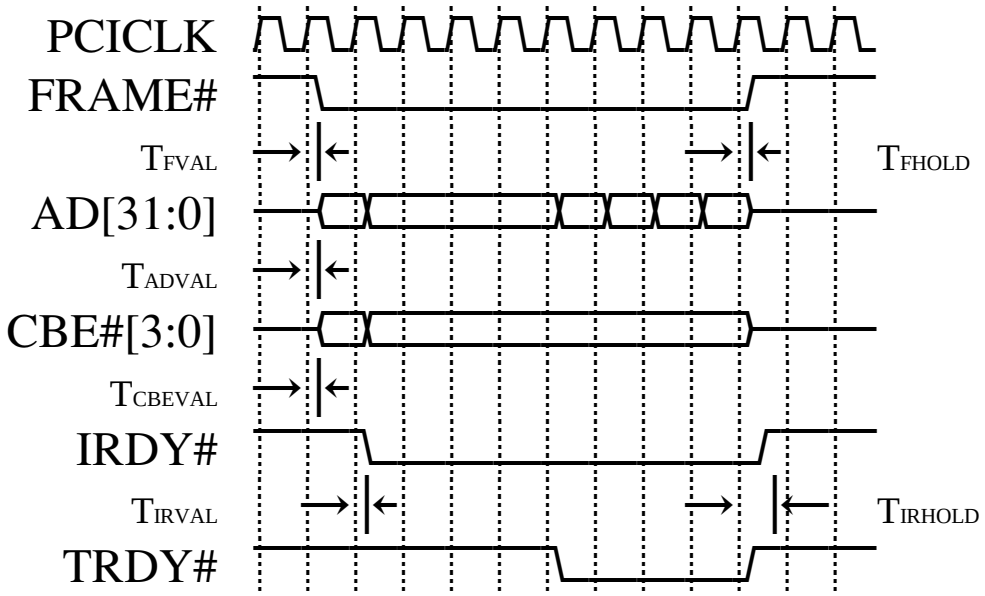
Figure 9 - Getting Transmit Descriptor



Symbol	Parameter	Width (ns)	Notes
T_{FVAL}	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
T_{ADVAL}	PCICLK rising edge to AD[31:0] Valid Delay	(8.6, 12.7, 22.3)	
T_{CBEVAL}	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
T_{IRVAL}	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.2)	
T_{FHOLD}	FRAME# hold time	(7.0, 10.3, 18.2)	2.
T_{IRHOLD}	IRDY# hold time	(3.2, 4.8, 8.4)	3.

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)
2.FRAME# hold time for frame#=0 to frame#=1
3.IRDY# hold time for frame#=0 to frame#=1

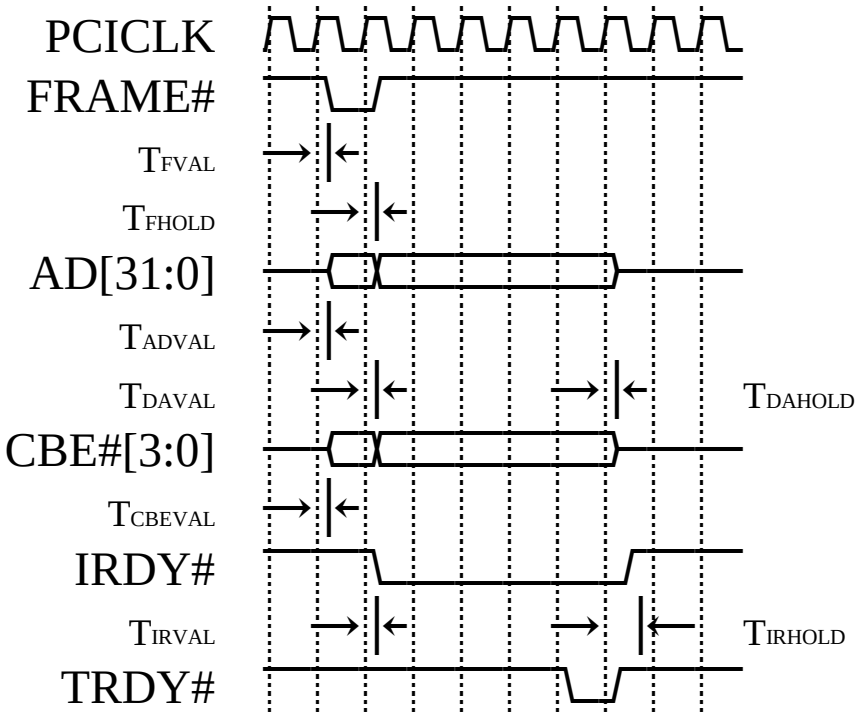
Figure 10 - Getting Receive Descriptor



Symbol	Parameter	Width (ns)	Notes
T_{FVAL}	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
T_{ADVAL}	PCICLK rising edge to AD[31:0] Valid Delay	min:(7.7, 11.1, 20.0), max:(8.6, 12.7, 22.3)	
T_{CBEVAL}	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
T_{IRVAL}	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.2)	
T_{FHOLD}	FRAME# hold time	(7.0, 10.3, 18.2)	2.
T_{IRHOLD}	IRDY# hold time	(3.2, 4.8, 8.4)	3.

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)
2.FRAME# hold time for frame#=0 to frame#=1
3.IRDY# hold time for frame#=0 to frame#=1

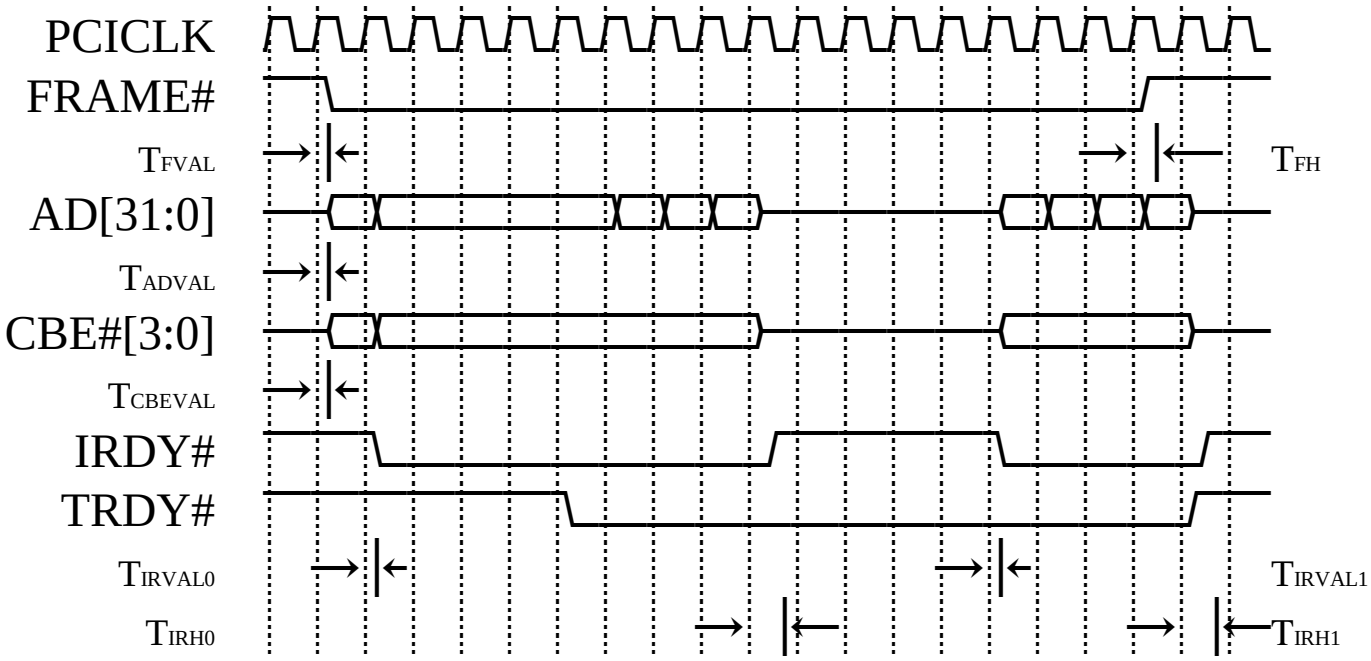
Figure 11 - Write Back Status to Descriptor



Symbol	Parameter	Width (ns)	Notes
TFVAL	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
TADVAL	PCICLK rising edge to AD[31:0] Valid Delay	(7.7, 11.4, 20.0)	
TCBEVAL	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
TIRVAL	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.3)	
TFHOLD	FRAME# hold time	(5.7, 8.4, 14.8)	
TDAVAL	PCICLK rising edge to AD[31:0](data) Valid Delay	(7.2, 10.6, 18.7)	
TFHOLD	FRAME# hold time	(5.7, 8.4, 14.8)	
TDAHOLD	AD[31:0] hold time	(5.2, 7.6, 13.4)	
TIRHOLD	IRDY# hold time	(3.2, 4.8, 8.4)	

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)

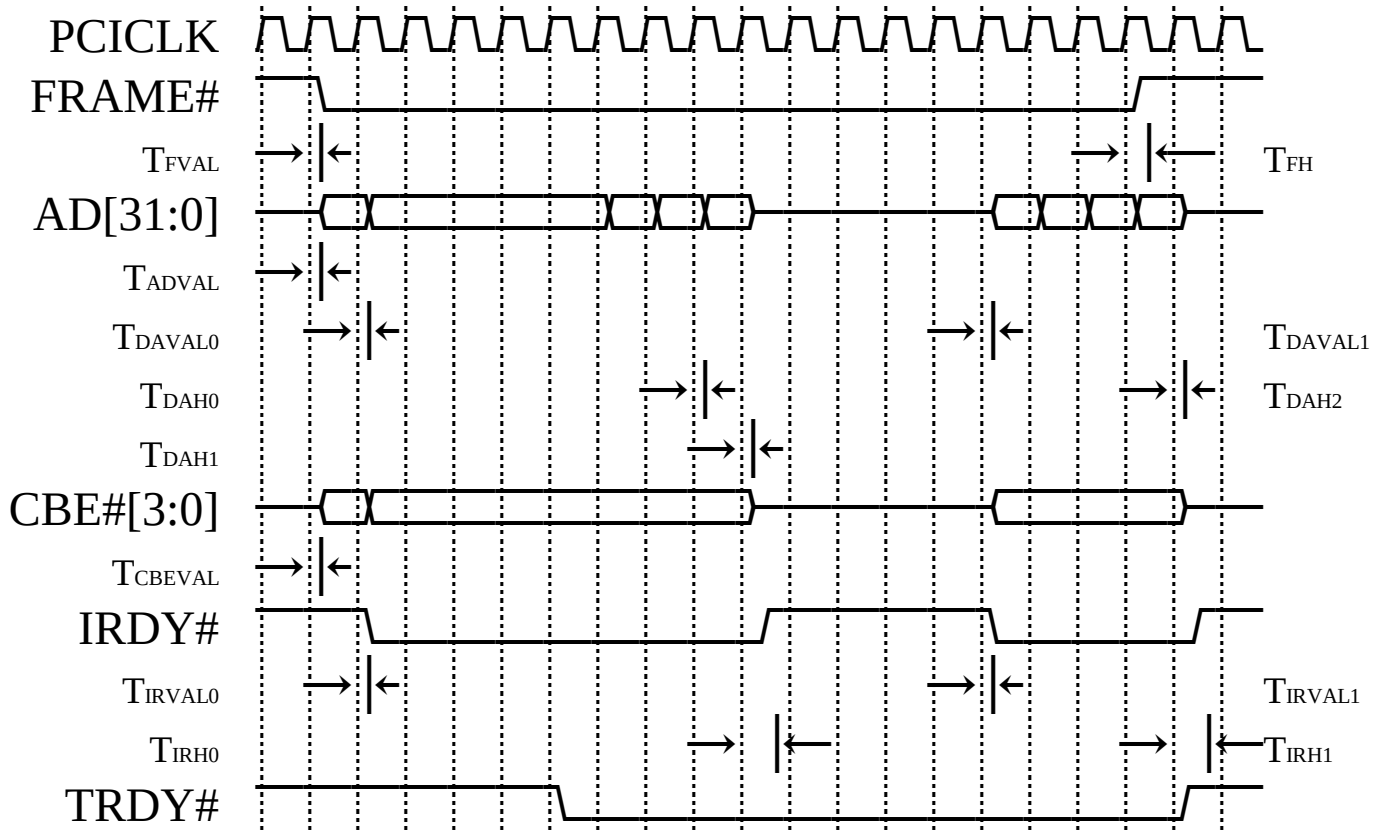
Figure 12 - Read Data into FIFO



Symbol	Parameter	Width (ns)	Notes
T_{FVAL}	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
T_{FH}	FRAME# hold time	(6.9, 10.2, 17.9)	
T_{IRVAL0}	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.3)	
T_{IRVAL1}	PCICLK rising edge to IRDY# Valid Delay	(4.8, 7.0,12.4)	
T_{IRH0}	IRDY# hold time	(3.5, 5.1, 8.9)	
T_{IRH1}	IRDY# hold time	(3.2, 4.8, 8.4)	
T_{ADVAL}	PCICLK rising edge to AD[31:0] Valid Delay	(9.5, 13.9, 24.5)	
T_{CBEVAL}	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.3)	

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)

Figure 13 - Write Data from FIFO

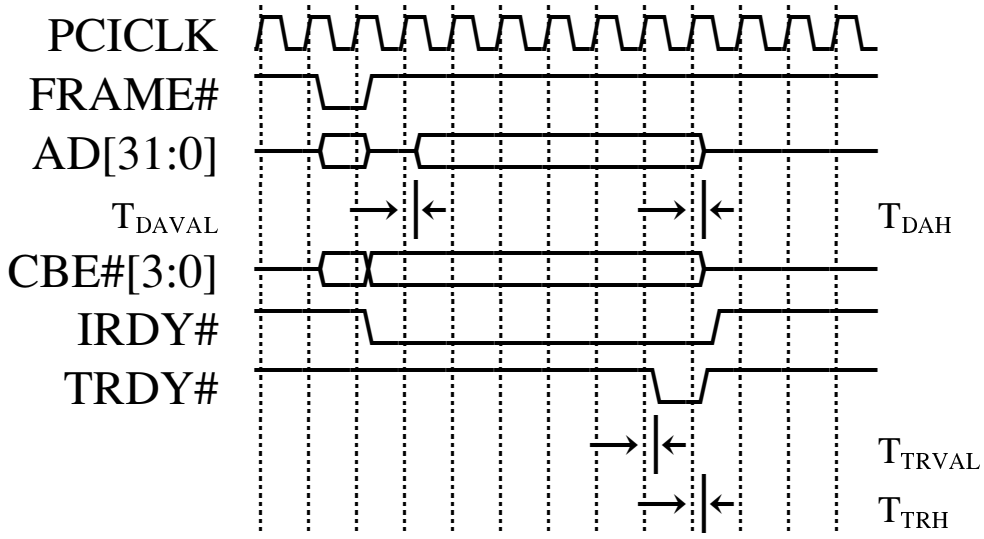


Symbol	Parameter	Width (ns)	Notes
T_{FVAL}	PCICLK rising edge to FRAME# Valid Delay	(7.2, 10.6, 18.7)	
T_{FH}	FRAME# hold time	(7.6, 11.2, 19.7)	
T_{IRVAL0}	PCICLK rising edge to IRDY# Valid Delay	(4.7, 7.0, 12.3)	
T_{IRVAL1}	PCICLK rising edge to IRDY# Valid Delay	(5.3, 7.9, 13.8)	
T_{ADVAL}	PCICLK rising edge to AD[31:0] Valid Delay	(9.5, 13.9, 24.5)	
T_{CBEVAL}	PCICLK rising edge to CBE[3:0] Valid Delay	(4.7, 7.0, 12.2)	
T_{IRH0}	IRDY# hold time	(4.0, 5.8, 10.3)	
T_{IRH1}	IRDY# hold time	(3.2, 4.8, 8.4)	
T_{DAVAL0}	PCICLK rising edge to data Valid Delay	(7.2, 10.6, 18.6)	
T_{DAVAL1}	PCICLK rising edge to data Valid Delay	(7.7, 11.1, 19.5)	
T_{DAH0}	Data hold time	(7.4, 10.9, 19.2)	
T_{DAH1}	Data hold time	(5.1, 7.6, 11.5)	
T_{DAH2}	Data hold time	(5.2, 7.9, 13.4)	

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)

PCI Bus Slave Cycles

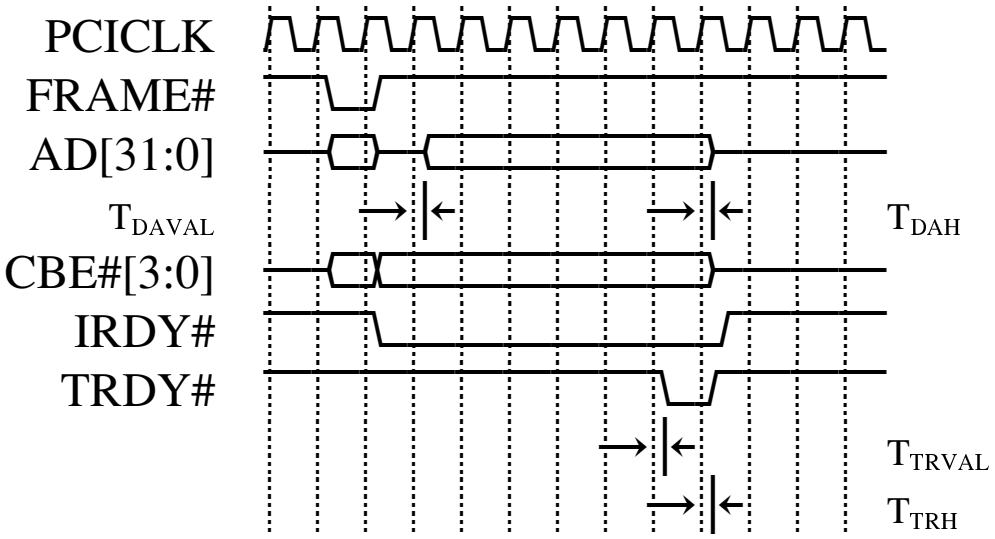
Figure 14 - IO Read/Write



Symbol	Parameter	Width (ns)	Notes
T_{DAVAL}	PCICLK rising edge to DATA Valid Delay	(8.2, 12.1, 21.3)	2
T_{DAH}	DATA hold time	(8.4, 12.1, 21.9)	2
T_{TRVAL}	PCICLK rising edge to TRDY# Valid Delay	(4.6, 6.7, 11.8)	
T_{TRH}	TRDY# hold time	(3.1, 4.6, 8.2)	

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)
2. IO read only

Figure 15 - Configuration Space Read/Write

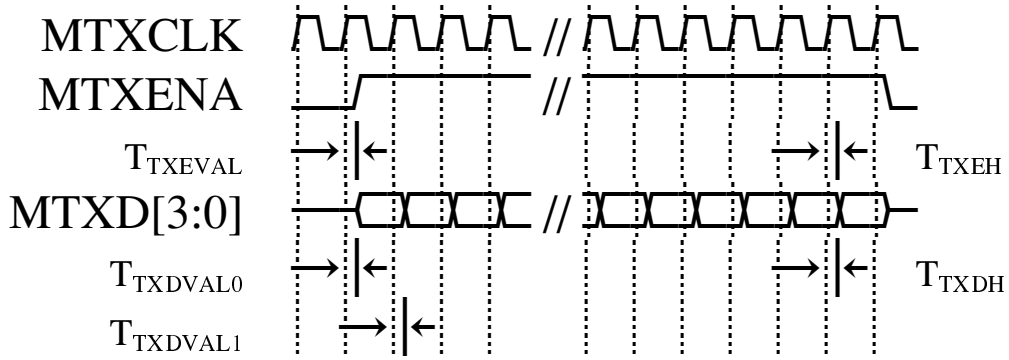


Symbol	Parameter	Width (ns)	Notes
T_{DAVAL}	PCICLK rising edge to DATA Valid Delay	(8.2, 12.1, 21.3)	2
T_{DAH}	DATA hold time	(5.8, 8.5, 15.0)	2
T_{TRVAL}	PCICLK rising edge to TRDY# Valid Delay	(4.6, 6.7, 11.8)	
T_{TRH}	TRDY# hold time	(3.1, 4.6, 8.2)	

Note :
1.(xxx, xxx, xxx) : (best, normal, worst)
2.Cfg read only

MII Timing Diagrams

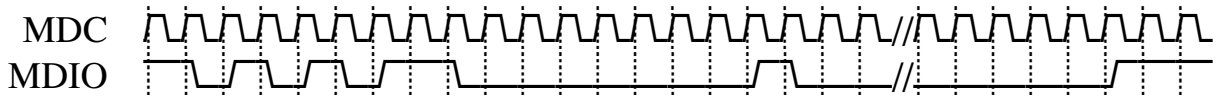
Figure 16 - MII Data Transmit



Symbol	Parameter	Width (ns)	Notes
T_{TXEVAL}	PCICLK rising edge to MTXENA Valid Delay	(3.7, 5.4, 9.5)	
$T_{TXDVAL0}$	PCICLK rising edge to MTXD Valid Delay	(3.6, 5.3, 9.3)	
$T_{TXDVAL1}$	PCICLK rising edge to MTXD Valid Delay	Min.(3.5, 5.1, 8.9) Max.(5.8, 8.6, 15.1)	
T_{TXEH}	MTXENA hold time	(5.9, 8.7, 15.3)	
T_{TXDH}	MTXD hold time	(5.7, 8.4, 14.7)	

Note:-
1.(xxx, xxx, xxx) : (best, normal, worst)

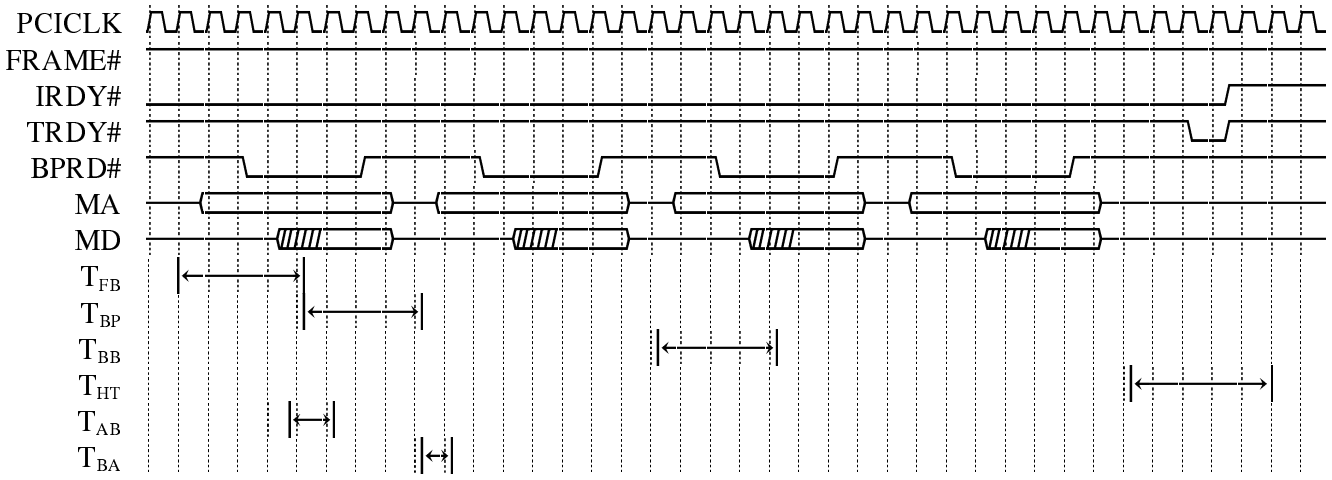
Figure 17 - Management Port Write



All MDIO signal transitions occur on the negative edge of MDC.

BootRom Timing

Figure 18 - One Dword Bootrom Access Timing (without Delay Transaction)

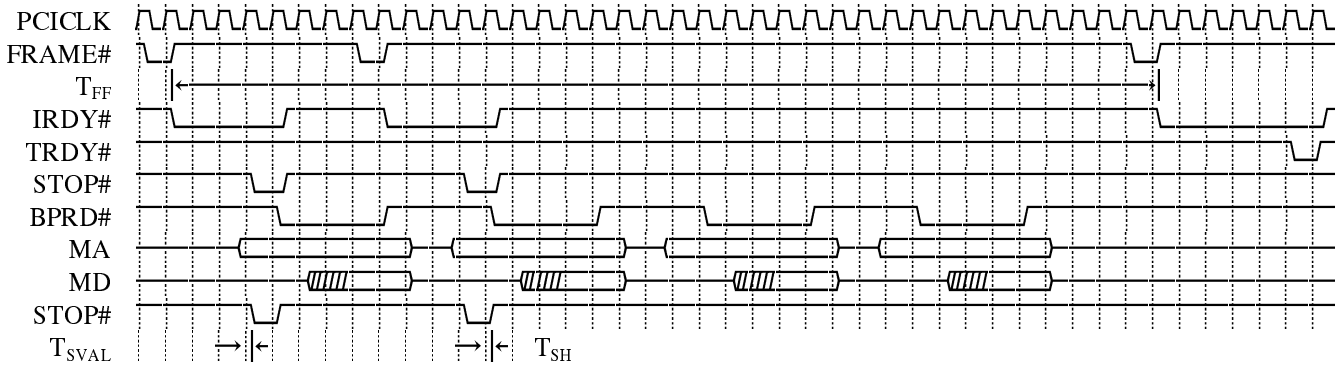


Symbol	Parameter	Min	Max	Notes
T_{FB}	PCICLK rising edge which latches FRAME# to BPRD# asserted		487	2
T_{AB}	MA ready to BPRD# asserted		29.4	
T_{BP}	BPRD# asserted	508 (DTSEL=1)	298 (DTSEL=0)	3
T_{BA}	BPRD# deasserted to MA deasserted		29.5	
T_{BB}	BPRD# deasserted between two one-byte bootrom cycles		511	
T_{BT}	BPRD# deasserted to PCICLK rising edge which latches TRDY#		143	

Note :

1. Delay transaction control bit : PCI cfg/7ah/bit5
2. DTSEL : PCI cfg/7ah/bit4

Figure 19 - One Dword Bootrom Access Timing (with Delay Transaction)



Symbol	Parameter	Width (ns)	Notes
T_{FF}	Initial FRAME# to Second Valid FRAME#	(3300, 3300, 3300)	
T_{SVAL}	PCICLK Rising Edge to STOP# Valid Delay	(5.4, 8.0, 14.1)	
T_{SH}	STOP# Hold Time	(3.8, 5.6, 9.8)	

PACKAGE MECHANICAL SPECIFICATIONS

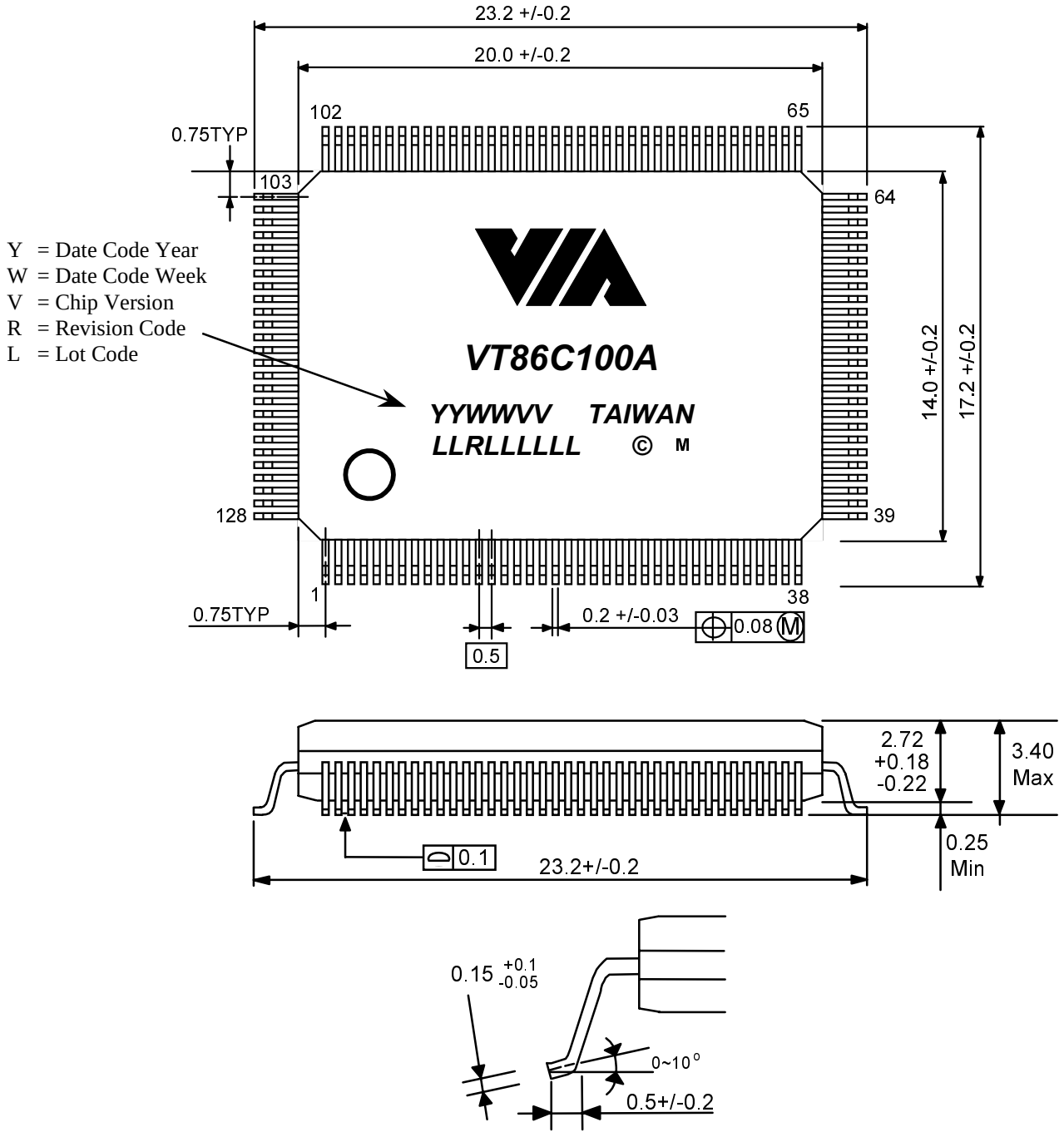


Figure 20. Mechanical Specifications – 128 Pin PQFP Package