VT6122

Gigabit Ethernet Controller

DATASHEET

Revision 1.6
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VIA Networking Technologies, Inc.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	2003-10-13	Initial release	SHC
1.1	2003-12-12	Modified values in Table 22 "Absolute Maximum Ratings" and in Table 23 "DC Specifications" Added Table 24 "Current Consumption"	SHC
1.2	2003-12-17	Modified Table 22 "Absolute Maximum Ratings"	SHC
1.3	2003-12-29	Modified Table 22 "Absolute Maximum Ratings"	SHC
1.4	2004-02-04	Revised the description of Pin 74, VEESEL	SHC
1.5	2004-04-16	Added product information markings and descriptions to the diagram in Figure 16, 128-Pin EP-LQFP Package, in the Mechanical Specifications section.	SHC
1.6	2004-05-21	Modified Table 16 "LED Select."	SHC

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Gigabit Ethernet Controller

PRODUCT FEATURES

- **Feature**
  - Fully IEEE 802.3 2002 compliant
  - Optional on-chip switching regulator circuit
  - Automatic detection and correction of cable pair swaps, pair skew, and pair polarity, along with an automatic MDI/MDI-X crossover function
  - Optional integrated oscillator circuit
  - Five direct-drive LED pins with four programmable LED modes
  - Low EMI line drivers with robust CESD performance
  - Manufactured in mainstream 3.3V/1.5V digital CMOS process
- **Bus Architecture.**
  - Compliance to PCI Rev. 2.2, 33/66 MHz, 32 bit
  - PCI Bus master Dual Channel DMA support for Tx/Rx
  - Tx/Rx descriptor Scatter and Gather support in host memory
  - No Transmit data byte alignment restriction; Rx data buffer should be double-word aligned
  - Flexible programmable Bus master burst sizes and advanced internal arbitration control to optimize the bus utilization
  - 256 bytes IO map/ 256 bytes memory map IO range in 32-bit addressing
  - 64-bit addressing option in EEPROM
    - Bus Master 64-bit addressing
    - Use global Descriptor DMA and FIFO DMA Hi-16 bit address
  - Adaptive interrupt service scheme for interrupt coalescence
- **Network Functionality**
  - 64 x 48 CAM for 32 perfect filtering and 32 interest packet-perfect filtering
  - 16 kilobyte jumbo frame support
  - Integrated 16 kilobyte (2048 × 64) TX FIFO, 48 kilobytes (6144 × 64) RXFIFO for high performance applications

- **Network Management**
  - WFM 2.0 enabled for server
  - SNMP management, DMI 2.0, PXE 2.1
  - ACPI, Wake On LAN, and Microsoft onNow
  - PCI PMU 1.1
  - 802.1Q VLAN, 64 × 12 CAM VLAN ID perfect filtering
  - Long frame support (1518 + 4)
  - VLAN tag insertion for transmit packets
  - VLAN tag detection and removal for receive packets
  - 802.1p four-level priority transmit. (MAC support 4 TD, 1 RD queue)
  - Checksum offload
    - IPv4 checksum task offload
    - IEEE 802.1Q compliant VLAN are supported
    - Fragmented IP datagrams are not supported
    - Tx checksum generation for IP (IP option), TCP, and UDP
    - Rx checksum validation for IP (IP option), TCP, and UDP
  - Statistics for RFC 1213 (MIB II) RFC 1398 (etherLike MIB) 802.3 LME
  - Large Packet Segmentation Offload
- **Miscellaneous Supports**
  - 16-word 93c46/93c06 serial ROM interface, support
    - Embedded random word access
    - Dynamic and power-up loading to update chip default configuration
    - Software-driven direct programming
  - Supports Shadow-EEPROM function to work without an external EEPROM device
    - Built-in 16-word shadow memory to store EEPROM data
  - Supports four modes of LED behaviors. (five LED pins)
  - Build-in power-switching regulator to simplify power partition on board
- **Advanced Software Support**
  - GigaCheck: NIC management application in Windows platform.
  - DMI-GE: DMI CI and MA in Windows platform
  - VSNMP-GE: SNMP extension agent in Windows platform
  - VeriPHY™ Link Management Suite: integrated into GigaCheck cable analysis and link analysis function
- **Technology**
  - 1.5V core power and 3.3V I/O power with 5V PCI tolerant inputs
  - 14 mm × 14 mm, 128-pin LQFP with 0.4 mm pin pitch
- **System Application**
  - Desktop NIC
  - LAN-on-Motherboard and Mobile PC NICs

OVERVIEW

VT6122 is a PCI Rev. 2.2 10/100/1000 MHz integrated single chip (MAC + PHY) for Network Interface Card (NIC) and LAN On Motherboard (LOM) applications. It is a high-performance network solution for workstations and servers, offering two gigabits per second of aggregated bandwidth. Support for the VT6122 includes critical performance and management related advanced features.

The VT6122 is fully compliant with PCI power management Rev. 1.1 and ACPI Rev. 1.0. It implements multiple wake-up events including magic packets, pattern-match packets, and link-status changes. The VT6122 also support AC power loss and PCI abnormal shut down wake up cases on Magic packet power management mechanisms.

The driver and silicon have been developed together to provide the optimal performance in term of both throughput and host CPU utilization.

The twisted pair interface includes an innovative internal hybrid and a very low EMI line driver with robust Cable Sourced ESD (CESD) performance, allowing the use of the lowest-cost 1:1 magnetic modules, minimum external components, and less complex PCB traces. To further reduce system complexity and cost, the VT6122 can optionally be powered from a single 3.3V power supply when utilizing the device's on-chip regulator control circuit to produce the 1.5V core power supply voltage.

The VT6122 leverages Cicada's proprietary MicroPHY™ DSP Technology, key to enabling an extremely low-power Gigabit PHY on a single chip. Cicada's mixed signal and DSP architecture yields robust performance, supporting both full- and half-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T Ethernet over unshielded twisted pair (UTP) cable, with more than 5 dB of design margin with respect to all worst- case impairments (NEXT, FEXT, Echo, and system noise). The industry's highest-performance, lowest-power DSP-based transceiver utilizes an optimum trellis decoding algorithm in concert with all digital gain control and timing recovery.

To enable maximum network management feedback to the host system and the user, VeriPHY™ Link Management Suite routines allow extensive network and cable plant operating and status information, such as the cable length and effective Bit Error Rate (BER) that greatly simplifies Gigabit Ethernet network deployment and management.

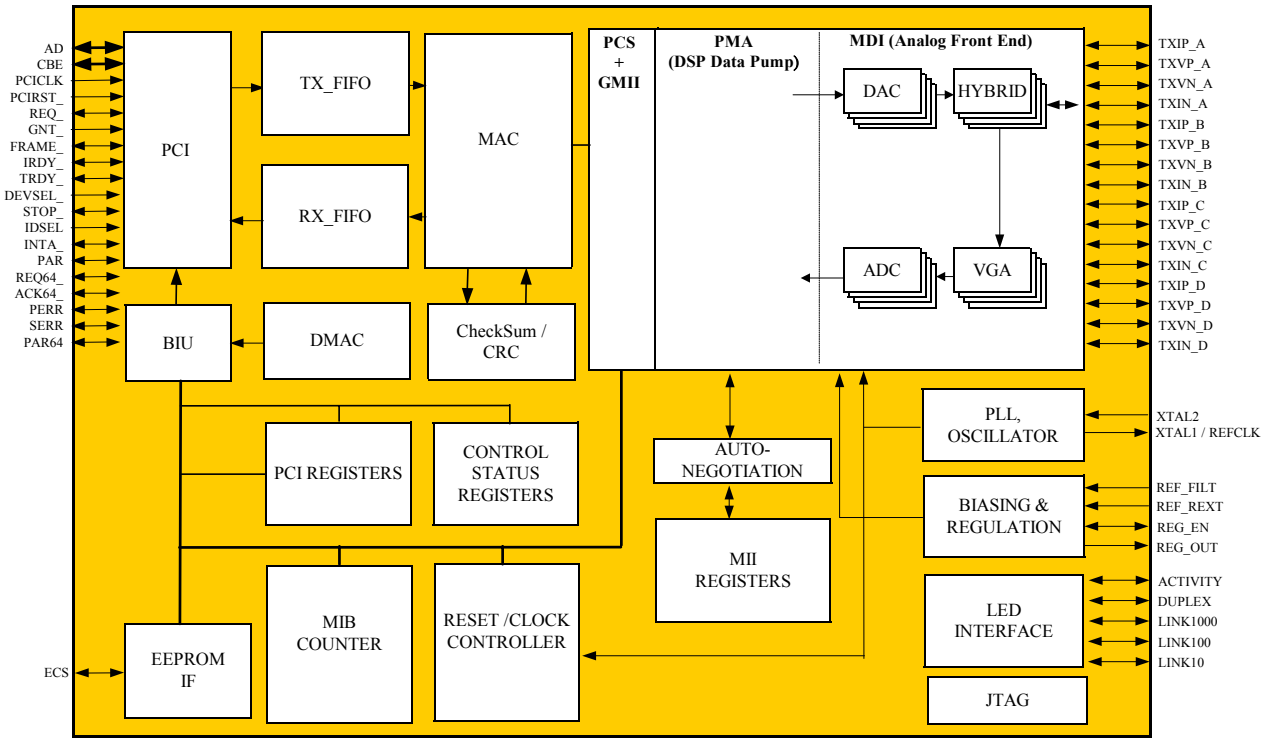


Figure 1. Internal Block Diagram

PINOUT

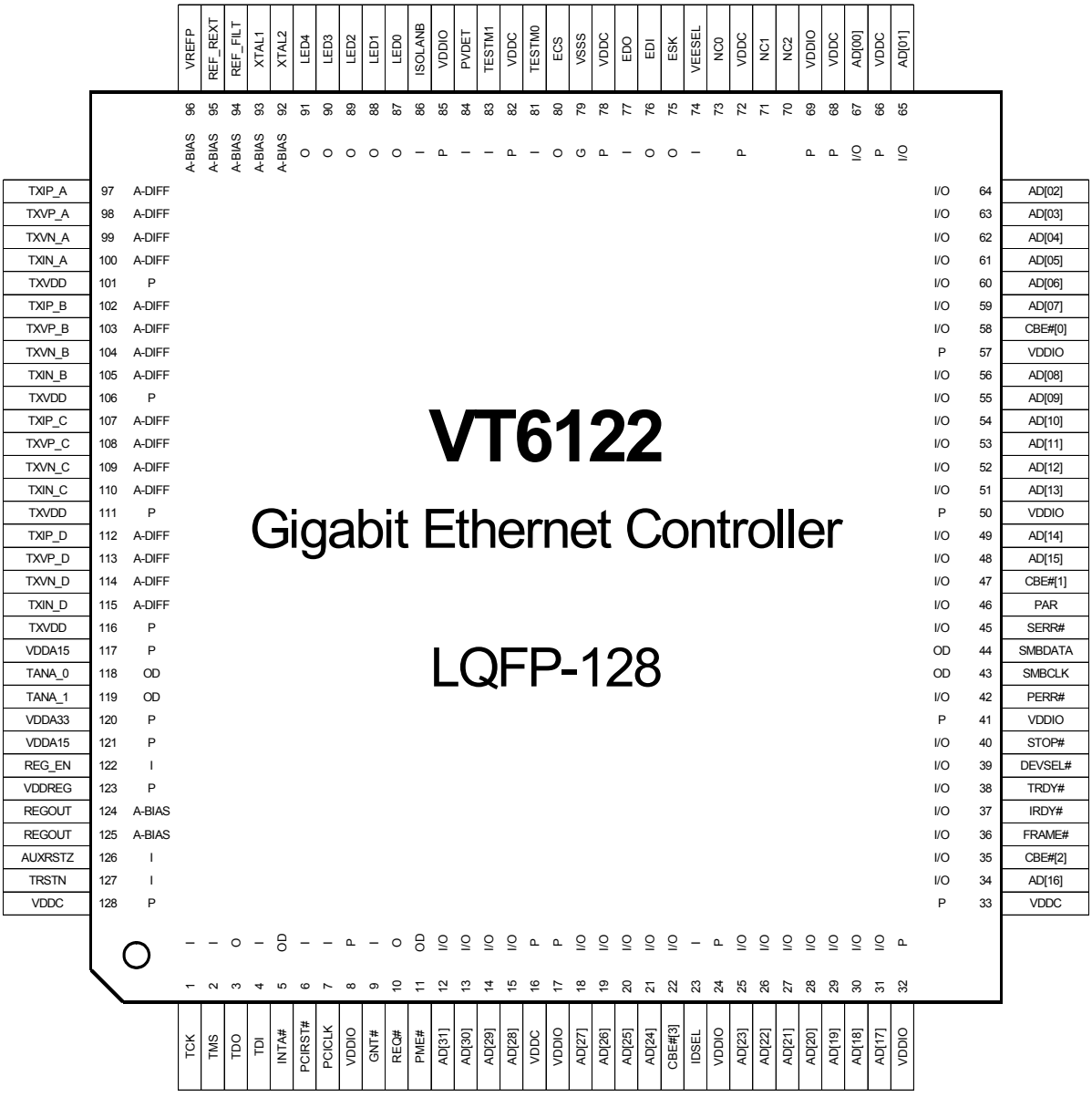


Figure 2. Pin Diagram

Table 1. Pin List

Name	No.	Type
AD[00]	67	I/O
AD[01]	65	I/O
AD[02]	64	I/O
AD[03]	63	I/O
AD[04]	62	I/O
AD[05]	61	I/O
AD[06]	60	I/O
AD[07]	59	I/O
AD[08]	56	I/O
AD[09]	55	I/O
AD[10]	54	I/O
AD[11]	53	I/O
AD[12]	52	I/O
AD[13]	51	I/O
AD[14]	49	I/O
AD[15]	48	I/O
AD[16]	34	I/O
AD[17]	31	I/O
AD[18]	30	I/O
AD[19]	29	I/O
AD[20]	28	I/O
AD[21]	27	I/O
AD[22]	26	I/O
AD[23]	25	I/O
AD[24]	21	I/O
AD[25]	20	I/O
AD[26]	19	I/O
AD[27]	18	I/O
AD[28]	15	I/O
AD[29]	14	I/O
AD[30]	13	I/O
AD[31]	12	I/O

Name	No.	Type
AUXRSTZ	126	I
CBE#[0]	58	I/O
CBE#[1]	47	I/O
CBE#[2]	35	I/O
CBE#[3]	22	I/O
DEVSEL#	39	I/O
ECS	80	O
EDI	76	O
EDO	77	I
ESK	75	O
FRAME#	36	I/O
GNT#	9	I
IDSEL	23	I
INTA#	5	OD
IRDY#	37	I/O
ISOLANB	86	I
LED0	87	O
LED1	88	O
LED2	89	O
LED3	90	O
LED4	91	O
NC0	73	
NC1	71	
NC2	70	
PAR	46	I/O
PCICLK	7	I
PCIRST#	6	I
PERR#	42	I/O
PME#	11	OD
PVDET	84	I
REF_FILT	94	A-BIAS
REF_REXT	95	A-BIAS

Name	No.	Type
REG_EN	122	I
REGOUT	124	A-BIAS
REGOUT	125	A-BIAS
REQ#	10	O
SERR#	45	I/O
SMBCLK	43	OD
SMBDATA	44	OD
STOP#	40	I/O
TANA_0	118	OD
TANA_1	119	OD
TCK	1	I
TDI	4	I
TDO	3	O
TESTM0	81	I
TESTM1	83	I
TMS	2	I
TRDY#	38	I/O
TRSTN	127	I
TXIN_A	100	A-DIFF
TXIN_B	105	A-DIFF
TXIN_C	110	A-DIFF
TXIN_D	115	A-DIFF
TXIP_A	97	A-DIFF
TXIP_B	102	A-DIFF
TXIP_C	107	A-DIFF
TXIP_D	112	A-DIFF
TXVDD	101	P
TXVDD	106	P
TXVDD	111	P
TXVDD	116	P
TXVN_A	99	A-DIFF
TXVN_B	104	A-DIFF

Name	No.	Type
TXVN_C	109	A-DIFF
TXVN_D	114	A-DIFF
TXVP_A	98	A-DIFF
TXVP_B	103	A-DIFF
TXVP_C	108	A-DIFF
TXVP_D	113	A-DIFF
VDDA15	117	P
VDDA15	121	P
VDDA33	120	P
VDDC	16	P
VDDC	33	P
VDDC	66	P
VDDC	68	P
VDDC	72	P
VDDC	78	P
VDDC	82	P
VDDC	128	P
VDDIO	8	P
VDDIO	17	P
VDDIO	24	P
VDDIO	32	P
VDDIO	41	P
VDDIO	50	P
VDDIO	57	P
VDDIO	69	P
VDDIO	85	P
VDDREG	123	P
VEESEL	74	I
VREFP	96	A-BIAS
VSSS	79	G
XTAL1	93	A-BIAS
XTAL2	92	A-BIAS

Table 2. Signal Type Definitions

Type	Description
I	**Input**. Input is a standard input-only signal.
O	**Output**. This is a standard active output driver.
I/O	**Input/Output**. This is an input/output signal
T/S	**Tri-State**. Tri-state is an inactive bi-directional input/output pin
OD	**Open Drain**. It allows multiple devices to share as a wire-OR.
A_{DIFF}	Analog differential signal pair for twisted pair interface.
A_{BIAS}	**Analog bias or reference signal**. Must be tied to external resistor and/or capacitor bias network, as shown in the system schematic in Figure 2.
P	**Power supply pin**
G	**Ground pin**

Table 3. Pin Descriptions

PCI Bus Interface			
Name	**Number**	**Type**	**Description**
AD[31:0]	See Table 1	I/O	**Address and Data**. Multiplexed address and data bus. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted.
PCIRST#	6	I	**PCI Reset.** When PCIRST# is asserted low, the chip performs an internal system hardware reset. PCIRST# may be asynchronous to PCICLK when asserted or de-asserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce-free edge.
PCICLK	7	I	**PCI Clock**. Provides timing for all transactions on PCI and is an input pin to every PCI device. The clock frequency range is from 0 to 66 MHz.
GNT#	9	I	**Bus grant**: Asserts to indicate to the device that access to the bus is granted.
IDSEL	23	I	**ID Select.** Used as a chip select during PCI configuration cycle.
INTA#	5	OD	**Interrupt** is an asynchronous signal which is used to request an interrupt
REQ#	10	O	**Bus request** is asserted by the bus master indicate to the bus arbiter that it wants to use the bus.
CBE#[3:0]	22 35 47 58	I/O	**Bus Command/Byte Enables:** are multiplexed on the same PCI pins. During the address phase of a transaction, CBE[3:0]# define the Bus Command. During the data phase, CBE[3:0]# are used as Byte Enables. The Byte Enables define which physical byte lanes carry meaningful data. CBE0# applies to byte 0 and CBE3# applies to byte 3.
PAR	46	I/O	**Parity** is even parity across AD31-0 and CBE3-0#. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.
FRAME#	36	I/O	**Frame**: Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in the final data phase.
IRDY#	37	I/O	**Initiator Ready** indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a write, IRDY# indicates that valid data is present on AD31-0. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
TRDY#	38	I/O	**Target Ready** indicates the target's agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a read, TRDY# indicates that valid data is present on AD31-0. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
DEVSEL#	39	I/O	**Device Select**. When actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
STOP#	40	I/O	**Stop**. The device drives STOP# to disconnect further transactions.
PERR#	42	I/O	**Parity error**. VT6122 as a master or target will assert this signal low when a data parity error is detected on any incoming data. As a master, it will monitor this signal on all write transactions.
SERR#	45	I/O	**System Error**. This signal is asserted low by VT6122 during address parity error and system errors if enabled.
SMBCLK	43	OD	**SMBus interface Clock signal**. Not available in VT6122.
SMBDATA	44	OD	**SMBus interface Data signal**. Not available in VT6122.

Power Management Interface			
Name	**Number**	**Type**	**Description**
PME#	11	OD	**Power management event.** This signal is asserted low to indicate a power management event has occurred.

Local Memory Interface			
Name	**Number**	**Type**	**Description**
VEESEL	74	I	**Virtual EEPROM Enable:** To enable the Virtual EEPROM function, this pin should be tied to LOW.
ESK	75	O	**EEPROM Clock:** External serial EEPROM clock
EDI	76	O	**EEPROM Data In:** External serial EEPROM data input.
EDO	77	I	**EEPROM Data Out:** External serial EEPROM data output.
ECS	80	O	**EEPROM Chip Select.** Chip select signal of the external EEPROM

Miscellaneous Interface			
Name	**Number**	**Type**	**Description**
TESTM0	81	I	Operation mode setting 0
TESTM1	83	I	Operation mode setting 1
AUXRSTZ	126	I	External RC for suspend power on reset for testing purpose
PVDET	84	I	Schmitt-trigger tied down input, used for global single power design approach to monitor PCI power.
ISOLAN#	86	I	Isolate LAN chip, active low.

Media Interface Signals			
Name	**Number**	**Type**	**Description**
TXIP_A	97	A_{DIFF}	**TX/RX Channel "A" positive hybrid pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1.
TXVP_A	98	A_{DIFF}	
TXIN_A	100	A_{DIFF}	**TX/RX Channel "A" negative hybrid pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "A" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2.
TXVN_A	99	A_{DIFF}	
TXIP_B	102	A_{DIFF}	**TX/RX Channel "B" positive hybrid pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3.
TXVP_B	103	A_{DIFF}	
TXIN_B	105	A_{DIFF}	**TX/RX Channel "B" negative hybrid pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "B" data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6.
TXVN_B	104	A_{DIFF}	
TXIP_C	107	A_{DIFF}	**TX/RX Channel "C" positive hybrid pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "C" data channel. In 1000 Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10M/100M modes).
TXVP_C	108	A_{DIFF}	
TXIN_C	110	A_{DIFF}	**TX/RX Channel "C" negative hybrid pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "C" data channel. In 1000 Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10M/100M modes).
TXVN_C	109	A_{DIFF}	
TXIP_D	112	A_{DIFF}	**TX/RX Channel "D" positive hybrid pair.** Positive differential pair connected to external termination resistors and then to the positive primary side of the transformer. This pin pair forms the positive signal of the "D" data channel. In 1000 Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10M/100M modes).
TXVP_D	113	A_{DIFF}	
TXIN_D	115	A_{DIFF}	**TX/RX Channel "D" negative hybrid pair.** Negative differential pair connected to external termination resistors and then to the negative primary side of the transformer. This pin pair forms the negative signal of the "D" data channel. In 1000 Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10M/100M modes).
TXVN_D	114	A_{DIFF}	

JTAG Interface			
Name	**Number**	**Type**	**Description**
TDI	4	I	**JTAG Test Data Serial Input.** Serial test pattern data is scanned into the device on this input pin, which is sampled with respect to the rising edge of TCK. This pin should be tied high during normal chip operation.
TDO	3	O	**JTAG Test Data Serial Output.** Serial test data is driven out of the device on the falling edge of TCK. This pin should be left floating during normal chip operation.
TMS	2	I	**JTAG Test Mode Select.** This input pin, sampled on the rising edge of TCK, controls the TAP (Test Access Port) controller's 16-state instruction state machine. This pin should be tied high during normal chip operation
TCK	1	I	**JTAG Test Clock.** This input pin is the master clock source used to control all JTAG test logic in the device. This pin should be tied low during normal chip operation.
TRST#	127	I	**JTAG Reset.** This active low input pin serves as an asynchronous reset to the JTAG TAP controller's state machine. As required by the JTAG standard, this pin includes an on-chip pull-up resistor. Alternatively, if the JTAG port of the device is not used on the printed circuit board, then this pin should be tied to ground (VSSIO) with a pull-down resistor.

LED Status Output			
Name	**Number**	**Type**	**Description**
LED[4:0]	87, 88, 89 90, 91	O	**LED Status Outputs.** Output pins for directly driving status LEDs. When enabled by MII register bit 27.3, all LED outputs are pulsed at 5 kHz with a 20% duty cycle for low-power operation.

System Clock Interface			
Name	**Number**	**Type**	**Description**
XTAL1/ REFCLK	93	I	**Crystal Input / Reference Clock Input.** The reference input clock can be 25 MHz, with a +50 ppm frequency tolerance or connected to a 25 MHz, parallel resonant crystal with a +50 ppm frequency tolerance. When used with a crystal, a 33 pF capacitor is connected from this pin to ground.
XTAL2	92	O	**Crystal Output.** 25 MHz parallel resonant crystal output. If the on-chip oscillator is enabled, a 33 pF capacitor is connected from this output to ground.

Regulator Control and Analog Bias Pins			
Name	**Number**	**Type**	**Description**
REF_REXT	95	A_{BIAS}	**Bias** pin to external 2.26k (1%) resistor tied to analog ground
REF_FILT	94	A_{BIAS}	**Reference Generator Filter** pin to external 1 µF (+/-10%) capacitor tied to analog ground.
VREFP	96	A_{BIAS}	**Positive Reference Bias.** Analog reference generator positive supply input. VREFP should be tied to analog 3.3V supply with a short signal trace. A 1 µF capacitor should be placed between VREFP and ground, as close to the device package as possible.
REG_EN	122	I	**Regulator Control Enable.** Active High input enables on-chip switching regulator in order to generate the 1.5V supply voltage. Includes on-chip 100 kΩ pull-up resistor to VDD
TANA_0	118	N/C	**Test Pin.** These pins are open drain, which are used for debugging only and should be no-connects in a custom design.
TANA_1	119	N/C	
REGOUT	124, 125	A_{BIAS}	**Regulator output.** Used to drive an external inductor and capacitor.
VDDREG	123	P	Switching regulator 3.3V supply

Analog Power Supply Signal Description			
Name	**Number**	**Type**	**Description**
TXVDD	101, 106 111, 116	P	**Line driver supply (3.3V)**
VDDA15	121, 117	P	**Power.** Analog 1.5V core power.
VDDA33	120	P	**Power.** Analog 3.3V core power.

Digital Power Supply Signal Description			
Name	**Number**	**Type**	**Description**
VDDIO	See Table 1	P	**I/O power supply (3.3V)**
VDDC	See Table 1	P	**Core power supply (1.5V)**
VSSS	79	G	**Core ground (0V)**
NC[2:0]	70, 71, 73		**No connect**

REGISTERS

Register Map Tables

PCI Configuration Space

Table 4. PCI Configuration Register Map

Byte 3	Byte 2	Byte 1	Byte 0	Offset (Hex)
Device ID (3119)		Vendor ID (1106)		00
STATUS (Bit 4=1)		COMMAND		04
CLASS_CODE (02_00_00)			Rev ID (10)	08
BIST (00)	Header type (00)	LAT Timer (R/W)	Cache Line (R/W)	0C
CSR IO Mapped Base Addr (256 Bt) 000			0 0 0 0 1	10
CSR MEM Mapped Base Addr (256 Bt) 000			0 0 0 0 0	14
32'h0000_0000				20
SUB System ID		SUB Vendor ID		2C
Expansion Rom Base Address 16		15 14 13 000000000000	E	30
24'h0			CAPABILITY (50)h	34
Max_LAT	Min_GNT	INT PIN (01)	4'h0 INTLN [3:0]	3C
Reserved				40-4F
PMU CAPABILITIES				
PMC(fr EE)		NIPTR(00)	01	50 h
DATA(00)	BSE(00)h	S 0000000 E	000000 WS[1]	54 h
	Waddr	VEE_Write_Port		58 h
VEE_CTL	Raddr	VEE_Read_Port		5C h
Reserved	Reserved	Reserved	Reserved	60 h
		Delay Timer		64 h

[1] WS: If software want to write a power state chip not support, the write cycle will be granted but discarded internally

MAC Registers Mapping Table

Listed in the table below are the abbreviations of register access types and its abbreviation implemented for the MAC registers.

Access Type	Description	Access Type	Description
RO	Read only	C/S	Clear or set by Hardware Controller
R0	Read as 0 always	R	Can be Read by software.
SC	Software Driver Control	W	Write by software
HC	Hardware Control	W0	Write “1” clear by software
E	Updated by EEPROM loading	W1	Write “1” set by software
U	Updated by Hardware Controller		

VT6122 provides 256 bytes space range with some page selection in some offset on PCI I/O Map and Memory mapped I/O space, defined in PCI configuration space 10h and 14h. In Windows and gigabit VGHCI, a memory mapped I/O based software is preferred. The I/O space addressing is defined to be 32-bit I/O read/write cycles.

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0	Type
00	PAR3	PAR2	PAR1	PAR0	RW/E
04	TCR	RCR	PAR5	PAR4	RW/E
08	CR3.S	CR2.s	CR1.s	CR0.s	RW1/E
0C	CR3.c	CR2.c	CR1.c	CR0.c	RW0/E
10	MAR3/CAM	MAR2/CAM	MAR1/CAM	MAR0/CAM	
14	MAR7/CAM	MAR6/CAM	MAR5/CAM	MAR4/CAM	
18	**DescBaseAddr.Hi[63:32]**				RW
1C	**Reserved**		**DataBufBaseAddr.Hi[63:48]**		RW
20	RXE_SR	TXE_SR	ISR_CTL		
24	ISR3	ISR2	ISR1	ISR0	RW0S
28	IMR3	IMR2	IMR1	IMR0	RW
2C	TD_STATUS_PORT				RW
30		RDCSR0.s[3:0]	TDCSR1.s	TDCSR0.s	RSU
34		RDCSR0.c[3:0]	TDCSR1.c	TDCSR0.c	RCU
38	RDBase0.Lo[31:6]				RW
3C	RQETMR	TQETMR	RDINDX		RWU
40	TDBase0.Lo[31:6]				RW
44	TDBase1.Lo[31:6]				RW
48	TDBase2.Lo[31:6]				RW
4C	TDBase3.Lo[31:6]				RW
50	TDCSIZE[11:0]		RDCSIZE		RW
54	TDIDX1[11:0]		TDIDX0[11:0]		RCU
58	TDIDX3[11:0]		TDIDX2[11:0]		RCU
5C	RBRDU		Tx Pause Timer		RW
60	Reserved				
64	Reserved				
68	Reserved	Reserved	CAMCR	CAMADDR	
6C	Reserved	PHYSR0	MIISR	MIICFG	
70	MII DATA PORT		MIIADR	MIICR	
74	SOFT TIMER 1		SOFT TIMER 0		RW
78	CFGD	CFGC	CFGB	CFGA	RWE
7C	MCFG1	MCFG0	DCFG1	DCFG0	RWE

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0	Type
80	STICKHW	PMCPORT	BISTSR	BISTCMD	
84	Reserved	Reserved	EE_SWDAT	MIBCR	
88	MIB READ PORT				
8C	BPMD_ w	Reserved	BPMA/EE_WR_DATA		
90	EECSR	CHKSUM	BPMD_r	BPCMD	
94	EMBCMD	EADDR	EE_RD_DATA		
98	MJMPSR	Reserved	CJMPSR	Reserved	
9C	CHIP_GCR	DEBUG	Reserved	CHIP_GSR	
A0	WOLCFG.s	PWCFG.s	WOLCR1.s	WOLCR0.s	RW1
A4	WOLCFG.c	PWCFG.c	WOLCR1.c	WOLCR0.c	RW0
A8	Reserved		WOLSR1.s	WOLSR0.s	RW1U
AC	Reserved		WOLSR1.c	WOLSR0.c	RW0
B0	PATTERN_CRC1[15:0]		PATTERN_CRC0[15:0]		RW
B4	PATTERN_CRC3[15:0]		PATTERN_CRC2[15:0]		RW
B8	PATTERN_CRC5[15:0]		PATTERN_CRC4[15:0]		RW
BC	PATTERN_CRC7[15:0]		PATTERN_CRC6[15:0]		RW
C0	Pattern 0/4, PTNBMSK[31:0]				RW
C4	Pattern 0/4, PTNBMSK[63:32]				RW
C8	Pattern 0/4, PTNBMSK[95:64]				RW
CC	Pattern 0/4, PTNBMSK[127:96]				RW
D0	Pattern 1/5, PTNBMSK[31:0]				RW
D4	Pattern 1/5, PTNBMSK[63:32]				RW
D8	Pattern 1/5, PTNBMSK[95:64]				RW
DC	Pattern 1/5, PTNBMSK[127:96]				RW
E0	Pattern 2/6, PTNBMSK[31:0]				RW
E4	Pattern 2/6, PTNBMSK[63:32]				RW
E8	Pattern 2/6, PTNBMSK[95:64]				RW
EC	Pattern 2/6, PTNBMSK[127:96]				RW
F0	Pattern 3/7, PTNBMSK[31:0]				RW
F4	Pattern 3/7, PTNBMSK [63:32]				RW
F8	Pattern 3/7, PTNBMSK [95:64]				RW
FC	Pattern 3/7, PTNBMSK [127:96]				RW

MII Register Mapping Table

Table 5. MII Registers Names & Addresses

Register Name	Register Number	Register Address (Hex)
Mode Control	0	00
Mode Status	1	01
PHY Identifier Register #1	2	02
PHY Identifier Register #2	3	03
Auto-Negotiation Advertisement	4	04
Auto-Negotiation Link Partner Ability	5	05
Auto-Negotiation Expansion	6	06
Auto-Negotiation Next-Page Transmit	7	07
Auto Negotiation Link Partner Next Page	8	08
1000BASE-T Control	9	09
1000BASE-T Status	10	0A
Reserved	11	0B
Reserved	12	0C
Reserved	13	0D
Reserved	14	0E
1000BASE-T Status Extension #1	15	0F
100BASE-TX Status Extension	16	10
1000BASE-T Status Extension #2	17	11
Bypass Control	18	12
Receive Error Counter	19	13
False Carrier Sense Counter	20	14
Disconnect Counter	21	15
10BASE-T Control & Status	22	16
Extended PHY Control #1	23	17
Extended PHY Control #2	24	18
Interrupt Mask	25	19
Interrupt Status	26	1A
Parallel LED Control	27	1B
Auxiliary Control & Status	28	1C
Delay Skew Status	29	1D
Reserved	30	1E
Reserved	31	1F

Table 6. MII Register Reset Sticky Bits

Register	Bit	Name
18	Bypass Control Register	
	6	Bypass Non-compliant BCM5400 Detection
	3	Parallel-Detect Control
	1	Disable Automatic 1000BASE-T Next-Page Exchange
	0	125MHz Clock Output Enable
22	10BASE-T Control & Status Register	
	15	Link Disable
	14	Jabber Detect Disable
	13	Disable 10BASE-T/100BASE-TX Echo Mode
	12	SQE Disable Mode
	11:10	Squelch Control
	5:3	Current Reference Trim
	2:1	CRS control
24	Extended PHY Control Register #2	
	15:13	100/1000BASE-T Edge Rate Control
	12:10	100/1000BASE-T Transmit Voltage Reference Trim
	9:7	TX FIFO Latency Control for GMII
	6:4	RTX FIFO Latency Control
25	Interrupt Mask Register	
	14	Speed State-Change Interrupt Mask
	13	Link State-Change/ActiPHY™ Interrupt Mask
	12	Duplex State-Change Interrupt Mask
	11	Auto-Negotiation Error Interrupt Mask
	10	Auto-Negotiation Done Interrupt Mask
	9	Page-Received Interrupt Mask
	8	Symbol Error Interrupt Mask
	7	Descrambler Lock-Lost Interrupt Mask
	6	MDI Crossover Interrupt Mask
	5	Polarity Change Interrupt Mask
	4	Jabber Detect Interrupt Mask
	3	False Carrier Interrupt Mask
	2	Parallel Detect Interrupt Mask
	1	Master/Slave Interrupt Mask
	0	10BASE-T RX_ER Interrupt Mask

Register	Bit	Name
27	LED Control Register	
	14	Link10 LED disable
	12	Link100 LED disable
	10	Link1000 LED disable
	8	Duplex LED disable
	6	Activity LED disable
	3	LED pulse enable
	2	Link/Activity LED Blink Enable
	1	Link/Activity LED Blink Rate

Remark: “Reset Sticky” refers to register bits that are not reset when a software reset is issued.

Register Description

MAC Registers

Offset 05h ~ 00h: PAR0 ~ PAR5 Ethernet Node Address Registers

Description: PAR5~PAR0 is Ethernet node ID, loaded from EEPROM while power on. PCI reset sequence is done or during software driven reload process. It also can be updated by software directly. The Node ID Registers are used as address filtering of incoming unicast packets.

Bit	Default	Type	Description
[47-0]	0	RWE	**PAR5~PAR0**. Ethernet node ID for unicast address filtering loaded from EEPROM at power up.

Offset 06h: Receive Control Register (RCR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	AS	AP	AL	PROM	AB	AM	AR	SEP

Bit	Default	Type	Description
7	0	RW	AS: Accept symbol error packet with good CRC. 1: Enable 0: Disable
6	0	RW	AP: Accept packet through perfect-filtering. Leave the receive type status to RD write-back status. 1: Enable 0: Disable
5	0	RW	AL: Accept long packet, 1518 / 1522(if contains 802.1p/802.1Q TAG) 1: Enable 0: Disable
4	0	RW	PROM: Promiscuous MODE. Accept all physical address packets 1: Enable 0: Disable
3	0	RW	AB: Accept Broadcast packet 1: Enable 0: Disable
2	0	RW	AM: Accept Multicast packet 1: Enable 0: Disable
1	0	RW	AR: Accept Runt packet 1: Enable 0: Disable
0	0	RW	SEP: Accept addressed packet with CRC error. 1:Enable 0: Disable

Offset 07h: Transmit Control Register (TCR)

Description: The TCR is reset by H_RESET and S_RESET

Bit Nbr	7	6	5	4	3	2	1	0
Func					COLTMC1	COLTMC0	LB1	LB0

Bit	Default	Type	Description
7	-	-	Reserved
6	-	-	Reserved
5	-	-	Reserved
4	-	-	Reserved
3-2	0h	RW	**COLTMC1, COLTMC0**: Collision retry control before aborting current transmission.
1-0	0h	RW	**LB1, LB0** : Internal/external loopback control

C1	C0	Description
0	0	Normal 16-times
0	1	2 sets, 32-times
1	0	3 sets, 48-times
1	1	Retry forever

LB1	LB0	Description
0	0	Normal
0	1	MAC Internal
1	0	External

Offset 08h: Global Command Register (CR0.s)

Bit Nbr	7	6	5	4	3	2	1	0
Func					TXON	RXON	STOP	STRT

Bit	Default	Type	Description
7-4	-	-	**Reserved**
3	0	-	**TXON**: Transmit process enable. 1: Enable 0: Disable
2	0	-	**RXON**: Receive process enable. 1: Enable 0: Disable
1	1	RW1	**STOP**: STOP NIC, reset STRT, default =1, set while Soft_Reset oo Hard_Reset 1: Enable 0: Disable
0	0	RW1	**STRT**: START NIC, being reset while STOP enabled or during Soft_Reset or Hard_Reset Before turning on TXON/RXON, STRT must be enabled.

Offset 09h: Global Command Register 1 (CR1.s)

Bit Nbr	7	6	5	4	3	2	1	0
Func	SFTRST	TM1EN	TM0EN	TDWBDIS	DPOLL	FDX	REAUTO	DISAU

Bit	Default	Type	Description
15	0	RW1C	**SFRST**: Software reset. Self-Cleared after internal logics reaching safe states
14	0	RW1	**TM1EN**: Enable periodic Software Timer counting
13	0	RW1	**TM0EN**: Enable single-shot Software Timer counting
12	-	-	**Reserved**
11	-	RW1	**DPOLL**: Disable Transmit and receive RD auto polling
10	-	-	**Reserved**
9	-	-	**Reserved**
8	-	RW1	**DISAU**. Unicast Reception Disable

Offset 0Ah: Global Command Register 2 (CR2.s)

Bit Nbr	7	6	5	4	3	2	1	0
Func	XONEN	FDX TFCEN	FDX RFCEN	HDX FCEN	XHITH1	XHITH0	XLTH1	XLTH0

Bit	Default	Type	Description
7	0	RW1	**XONEN**. IEEE 802.3x, XON/XOFF mode enable 1: NIC will transmit XON frame (Pause Timer = 16'h0000) as local Tx Pause Frame expired. **0**: Never transmit XON frame always.
6	0	RW1	**FDXTFCEN**. Full-duplex flow control TX enabled.
5	0	RW1	**FDXRFCEN**. Full-duplex flow control RX enabled
4	0	RW1	**HDXFCEN**. Half-duplex flow control enabled
3-2	'h0	RW	**XHITH1, XHITH0**. Transmit XON frame high threshold. **XHITH1** / **XHITH0** / Description 0 / 0 / 24 (default value) 0 / 1 / 32 1 / 0 / 48 1 / 1 / 64
1-0	'b11	RW	**XLTH1, XLTH0**. Transmit pause frame Low threshold. **XLTH1** / **XLTH0** / Description 0 / 0 / 4 0 / 1 / 8 1 / 0 / 16 1 / 1 / 24 (default value)

Offset 0Bh: Global Command Register 3 (CR3.s)

Bit Nbr	7	6	5	4	3	2	1	0
Func	Reserve	FORS RST	FPHYRST	DIAG		INTPCTL	GintMsk1	SWPEND

Bit	Default	Type	Description
7	0	RW1	Reserved
6	0	RW1	FOSRST**. Force exit Software stop without waiting for safe state**
5	0	RW1	FPHYRST**. Software generated to force PHYRSTZ active. For diagnosis purpose only.**
4	0	RW	DIAG**:. Diagnostic enabled.**
3	-	RW1	Reserved
2	0	RW1	INTPCTL**. Enable interrupt pending hold-off timer control** **0: No timer based interrupt pending control** **1: enable interrupt hold-off pending control**
1	0	RW1	GintMsk1**. Global Interrupt Mask 1. Disable INTA# generation from all ISR bits**
0	0	RW1	SWPEND. **Software based interrupt pending control. Disable INTA# generation from multi-level ISR bits defined in ISRCTL.PMSK[1:0]**

Offset 0Fh ~0Ch: Command Register Clear Port

Bit	Default	Type	Description
31-0	0	RW0	CR3.c, CR2.c, CR1.c, CR0.c Write "1" to clear the indexed register bit in command set port and clear.

Offset 17h ~ 10h: MultiCast Hashing Table Register

Offset 0x17h ~0x10h are shared with address recognition logic. MAR7~MAR0 are put on page 0 for 64-bit hashing table of multicast filtering. The mask bits of Address perfect filtering CAM and VLAN ID CAM are put on page 1. The data of Address perfect filtering CAM and VLAN ID CAM are put on page 2. The page definition is controlled by PS1, PS0 bit in 0x69h, CAMCR, bit7 and bit6. (PS1, PS0) = (0,0) is for MAR port, while (PS1, PS0)=(0,1) is for CAM Mask port and (PS1, PS0)=(1,0) is for CAM Data port.

In Summary,

1. Support 64-bit multicast hashing enable MAR0~MAR7
2. Support 64-bit address perfect filtering enable masks, and 64-bit VLAN ID perfect filtering enable masks

A_CAM data : {CAM5,CAM4,CAM3,CAM2,CAM1,CAM0}
V_CAM data : {CAM1,CAM0}
A_CAM mask: {CAM7,CAM6,CAM5,CAM4,CAM3,CAM2,CAM1,CAM0}
V_CAM mask: {CAM7,CAM6,CAM5,CAM4,CAM3,CAM2,CAM1,CAM0}

Description: **MAR7h~MAR0h** is the MAR Registers used to do multicast packets address filtering.

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
10	MAR3/CAM3	MAR2/CAM2	MAR1/CAM1	MAR0/CAM0
14	MAR7/CAM7	MAR6/CAM6	MAR5/CAM5	MAR4/CAM4

Bit	Default	Type	Description
63-0	'h0	RW	MAR7~MAR0**. 64-bit hashing table**

Offset 17h ~ 10h: . PCAM/VCAM Data and Mask Register

Description: **CAM7 ~ CAM0**. Accessed by CAM embedded Control and Data Port.

Bit	Default	Type	Description
63-0	'h0	RW	CAM7~CAM0**. 64-bit hashing table**

Offset 1Bh ~ 18h: Tx/Rx Descriptor Base Address High Register

Description: Tx/Rx Descriptor Higher 32-bit common address. Program it to required value if setup in 64-bit address environment, or leave it to be 0h for 32-bit address environment. While in 64-bit address environment, all descriptors use the same common high 32-bit address base.

Bit	Default	Type	Description
31-0	'h0	RW	Rx/Rx Descriptor Base Address High Register

Offset 1Dh ~ 1Ch: Tx/Rx Common Data Buffer Base Address High Register

Description: The Higher 16-bit common address of data buffer linked by Tx/Rx Descriptor. Program it to required value if setup in 64-bit environment, or leave it bo be 0'h for 32-bit address environment

Bit	Default	Type	Description
15-0	'h0	RW	Tx/Rx Common Data Buffer Base Address High Register

Offset 21h ~ 20h: Interrupt Control 0, 1 Register

Description: Interrupt Control by Software using hardware timer, the pending control only masks the interrupt source from UDPINT, PRXI, PTX0~3I.

Turns on CR3.INTPCTL will enable the interrupt pending control. Either SC_RELOAD or HC_RELOAD will has hardware reload the INTHOTMR and start to count down. Before INTHOTMR expired, all the interrupt events will be pending. When the count down process reaches zero, the INT_pending bit will be cleared to "0" and INA# issued if any interrupt event pended during this period. The interrupt pending process could be stopped any time by clearing the CR3.INTPCTL bit.

Bit Nbr	15	14	13	12	11	10	9	8
Func	UDPINT	TSUPDIS	RSUPDIS	PMSK1	PMSK0	INTPD	HRRLD	SCRLD
Bit Nbr	7	6	5	4	3	2	1	0
Func	SUPPTHR	SUPPTHR	SUPPTHR	SUPPTHR	SUPPTHR	SUPPTHR	SUPPTHR	SUPPTHR

Bit	Default	Type	Description
15	0	R0W	UDPINT.s**. User define interrupt set port, always read as 0.**
14	0	RW	TSUPP_DIS**. Disable Tx interrupt suppression feature.**
13	0	RW	RSUPP_DIS**. Disable Rx interrupt suppression feature.**
12-11	0	RW	PMSK1,0**. Interrupt masks selection bits for multiple levels interrupt control** **PMSK1** / **PMSK0** / Description 0 / 0 / Mask Layer-0 events 0 / 1 / Mask Layer-1 events 1 / 0 / Mask all interrupt events 1 / 1 / Mask all interrupt events
10	0	ROC	INT_Pending**. Hardware hold-off Interrupt Pending status.**
9	0	RW	HC_RELOAD**. While enabled, interrupt hold timer will be reload as ISR2.HFLD toggled.**
8	0	RW	SC_RELOAD**. While ISRCTL.HC_RELOAD is disabled, toggle this bit will reload the ISRCTL.INTHOTMR into interrupt hold timer.**
7-0	‘h0	RW	Page selector {**PS1, PS0**} **0 0** / **0 1** / **1 0** INTHOTMR / TSUPPTHR / RSPPTHR **INTHOTMR.** Programmable Interrupt Hold Timer. It will be loaded into internal interrupt hold timer as a start value through different ways (HC_RELOAD/SC_RELOAD). Before INTHOTMR expired, all those interrupt events will be held. This is a timer based adaptive interrupt scheme. The counter resolution is 20us and enabled while CR3.INTPCTL set to 1. **TSUPPTHR**. Tx interrupt-suppression threshold register. While tx int-suppr enabled (TSUPPD=0), the ***served tx packet*** will be counted one by one. Once the served number equals to this threshold register, high priority interrupt (PPTXI) will be set. RSUPPTHR**. Rx interrupt-suppression threshold register. While rx int-supp enabled (RSUPPD=0), the *served RD* will be counted one by one. Once the served RD number equals to this threshold register, high priority interrupt (PPRXI) will be se**t.

*Note***:**

GintMsk0 is in CR2[18], GintMsk1=CR2[19], INTPCTL in CR2[19].

Clear INTPCTL will release hold-off pending control immediately.

Multiple level Interrupt pending control is controlled by PMSK[1:0].

Layer-0	ISR0 : PTXnI, PRXI,PTXI. ISR1 : FLONI. ISR2 : UDPI,PWEI ISR3 : ISRn
Layer-1	Layer-0 + ISR0 : PPRXI, PPTXI.
Layer-2	all
Layer-3	all

Offset 22h: Transmit Host Error Status Register (TXE_SR)

Description: While ISR2.TXSTLI active, this register shows the detail error status. One or more bits in TDCSR.DEAD3, TDCSR.DEAD2, TDCSR.DEAD1, TDCSR.DEAD0 will be active also to indicate which Tx channel is involved.

Bit Nbr	7	6	5	4	3	2	1	0
Func					TFDBS	TDWBS	TDRBS	TDSTR

Bit	Default	Type	Description
7-4	0	R0	**ZeroBit**.
3	0	RW0S	**TFDBS**. Transmit FIFO DMA bus error
2	0	RW0S	**TDWBS**. TD write back host bus error
1	0	RW0S	**TDRBS.** TD descriptor fetch host bus error
0	0	RW0S	**TDSTR.** TD Structure Error. (1) TD link structure error. (2) Valid buffer segment (CMDZ) with zero buffer length.

Offset 23h: Receive Host Error Status Register (RXE_SR)

Description: While ISR3.RXSTLI active, this register shows the detail error status. The bit in RDCSR will also be active

Bit Nbr	7	6	5	4	3	2	1	0
Func					RFDBS	RDWBS	RDRBS	RDSTR

Bit	Default	Type	Description
7-4	0	R0	ZeroBit**.**
3	0	RW0S	RFDBS**. Rx FIFO DMA experience Host bus error.** **Write 1: clear the bit,** **Write 0: remain unchanged.**
2	0	RW0S	RDWBS**. RD write back host bus error** **Write 1: clear the bit,** **Write 0: remain unchanged.**
1	0	RW0S	RDRBS.**RD Fetch host bus error.** **Write 1: clear the bit,** **Write 0: remain unchanged.**
0	0	RW0S	RDSTR. **RD Structure Error.** **Write 1: clear the bit** **Write 0: remain unchanged.**

Offset 27h ~ 24h are the interrupt status registers. The interrupt event source bits are arranged to meet the Interrupt service hierarchy to maintain an efficient searching and programming methodology

Offset 24h: Interrupt Status Register 0 (ISR0)

Description: ISR0 shows service complete events of transmission and reception.

Bit Nbr	7	6	5	4	3	2	1	0
Func	PTX3I	PTX2I	PTX1I	PTX0I	PTXI	PRXI	PPTXI	PPRXI

Bit	Default	Type	Description
7-4	'h0	RW0S	**PTX3,2,1,0I**:Transmit service Complete staus in TD queue #3,2,1,0, Write 1 to clear this bit Write 0 to remain unchanged
3	0	ROS	**PTXI**. Combination results of PTXnI, Read Only
2	0	RW0S	**PRXI**. Receive Service complete, Write 1 to clear this bit Write 0 to remain unchanged
1	0	RW0S	**PPTXI**. High priority transmit interrupt Service Request. PTXn will be also set. Write 1 to clear this bit Write 0 to remain unchanged.
0	0	RW0S	**PPRXI**. High priority receive interrupt Service Request. PRXI will be also set Write 1 to clear this bit Write 0 to remain unchanged.

Offset 25h: Interrupt Status Register 1 (ISR1)

Bit Nbr	7	6	5	4	3	2	1	0
Func	SRCI	LSTPEI	LSTEI	OVFI	FLONI	RACEI	Reserved	Reserved

Bit	Default	Type	Description
7	0	RW0S	**SRCI**. Port Status Change Write 1 to clear this bit Write 0 to remain unchanged
6	0	RW0S	**LSTPEI**. Warning for RD List using up. LSTPEI is available only when TX flow control is enabled. Write 1 to clear this bit Write 0 to remain unchanged
5	0	RW0S	**LSTEI**. Receive Descriptor (RD) is used up Write 1 to clear this bit Write 0 to remain unchanged
4	0	RW0S	**OVFI.** Receive FIFO overflow. Some receive packets might be lost in this case. Write 1 to clear this bit Write 0 to remain unchanged
3	0	RW0S	**FLONI.** Indicate that a pause frame is received and flow control mechanism is enabled. Write 1 to clear this bit Write 0 to remain unchanged
2	0	RW0S	**RACEI.** The packet count queue of Receive FIFO overflow. Write 1 to clear this bit Write 0 to remain unchanged
1	0	RW0S	**Reserved**
0	0	RW0S	**Reserved**

Offset 26h: Interrupt Status Register 2 (ISR2)

Bit Nbr	7	6	5	4	3	2	1	0
Func	HFLD	UDPI	MIBFI	SHDNI	PHYI	PMEI	TMR1I	TMR0I

Bit	Default	Type	Description
7	0	R0W1	**HFLD.** Write 1 to enable hold off timer reload. Read as 0 always
6	0	RW0S	**UDPI**. User defined, software driven interrupt for diagnosis. Write 1 to clear this bit Write 0 to remain unchanged
5	0	RW0S	**MIBFI**. MIB counter near full.warning, Write 1 to clear this bit Write 0 to remain unchanged.
4	0	RW0S	**SHDNII**. Software shut down complete. Write 1 to clear this bit Write 0 to remain unchanged
3	0	RW0S	**PHYI.** While PHYINTEN is enabled, this bit shows phy interrupt event occurred.
2	0	RO	**PWEI**. Wake up power events reporting status for test purpose
1	0	RW0S	**TMR1I**. Programmable software Timer 1 expired interrupt status. Write 1 to clear this bit Write 0 to remain unchanged
0	0	RW0S	**TMR0I**. Programmable software Timer 0 expired interrupt status. Write 1 to clear this bit Write 0 to remain unchanged.

Offset 27h: Interrupt Status Register 3 (ISR3)

Description: ISR3 shows the comginations of other interrupt source.. This register is read only. To clear the interrupt, it is necessary to write clearing related source.

Bit Nbr	7	6	5	4	3	2	1	0
Func	ISR3	ISR2	ISR1	ISR0	Reserve	Reserve	TXSTLI	RXSTLI

Bit	Default	Type	Description
7-4	0	RO	**ISRn.** Interrupt Source indication. Read only
3	0	RO	**RESVI.** Read Only.
2	0	RO	**RESVI.** Read Only
1	0	RO	**TXSTLI.** Transmission DMA stall in TXE_SR. read only
0	0	RO	**RXSTLI.** Receive DMA Stall in RXE_SR. read only

Offset 2Bh ~ 28h: Interrupt Enable (Mask) Register 0, 1, 2, 3 (IMR0 ~ 3)

Description: Interrupt enable of ISR0 ~ISR3.

Bit Nbr	31	30	29	28	27	26	25	24
Func	PTX3M	PTX2M	PTX1M	PTX0M	PTXM	PRXM	PPTXM	PPRXM
Bit Nbr	23	22	21	20	19	18	17	16
Func	SRCM	LSTPEM	LSTEM	OVFM	FLONM	RACEM	Reserved	Reserved
Bit Nbr	15	14	13	12	11	10	9	8
Func	Reserved	UDPI	MIBFM	SHDNM	PHYM	PMEM	TMR1M	TMR0M
Bit Nbr	7	6	5	4	3	2	1	0
Func	ISR3M	ISR2M	ISR1M	ISR0M	Reserve	Reserve	TXSTLM	RXSTLM

Bit	Default	Type	Description
31-0	‘h0	RW	**IMRn.** Interrupt source enable control.

Offset 31h ~ 30h: Tx Descriptor Control Status Registers Set (TDCSRx.s)

Bit Nbr	15	14	13	12	11	10	9	8
Func	DEAD3	WAK3	ACT3	RUN3	DEAD2	WAK2	ACT2	RUN2
Bit Nbr	7	6	5	4	3	2	1	0
Func	DEAD1	WAK1	ACT1	RUN1	DEAD0	WAK0	ACT0	RUN0

Bit	Default	Type	Description
15	0	RWS	**DEAD3.** Indicate TD queue #3 encounters error conditions. (Set by HW / Reset by SW)
14	0	RWC	**WAK3.** Wake up TD queue #3 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
13	0	RU	**ACT3.** Indicating the end of TD queue #3T has not been reached when processing descriptors. (Set and Reset by HW)
12	0	RW	**RUN3.** Enable TD queue #3 operation. (Set and Reset by SW)
11	0	RWS	**DEAD2.** Indicate TD queue #2 encounters error conditions. (Set by HW / Reset by SW)
10	0	RWC	**WAK2.** Wake up TD queue #2 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
9	0	RU	**ACT2.** Indicate the end of TD queue #2 has not been reached when processing descriptors. (Set and Reset by HW)
8	0	RW	**RUN2.** Enable TD queue #2 operation.(Set and Reset by SW)
7	0	RWS	**DEAD1.** Indicate TD queue #1 encounters error conditions. (Set by HW / Reset by SW)
6	0	RWC	**WAK1**. Wake up TD queue #1 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
5	0	RU	**ACT1**. Indicate the end of TD queue #1 has not been reached when processing descriptors. (Set and Reset by HW)
4	0	RW	**RUN1**. Enable TD queue #1 to operation. (Set and Reset by SW)
3	0	RWS	**DEAD0**. Indicate TD queue #0 encounters error conditions.(Set by HW / Reset by SW)
2	0	RWC	**WAK0**. Wake up TD queue #0 to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
1	0	RU	**ACT0**. Indicate the end of TD queue #0 has not been reached when processing descriptors. (Set and Reset by HW)
0	0	RW	**RUN0**. Enable TD queue #0 to operate.(Set and Reset by SW)

Offset 35h ~ 34h: Tx Descriptor Control Status Register Clear (0x34-0x35h,TDCSRx.c)

Description: Write 1 will clear related TDCSR bit and won't take effect if write 0 on these bits

Bit	Default	Type	Description
15-8	0	RW0	**Bit definitions are the same as TDCSR1.s(0X31h).**
7-0	0	RW0	**Bit definitions are the same as TDCSR0.s(0X30h).**

Offset 33h ~ 32h: Rx Descriptor Control Status Register 0 Set (RDCSR.s)

Description: Write 1 will set RDCSR bits and will not take effect if write 0.

Bit Nbr	15	14	13	12	11	10	9	8
Func								

Bit Nbr	7	6	5	4	3	2	1	0
Func					DEAD	WAK	ACT	RUN

Bit	Default	Type	Description
15-8	0	R0	**Reserved**
7-4	0	R0	**ZeroBits**
3	-	RWS	**DEAD.** Indicate current queue encounters error conditions. (Set by HW / Reset by SW)
2	-	RWC	**WAK.** Wake RD queue to see if there is unprocessed descriptor. (Set by SW / Reset by HW)
1	-	RU	**ACT.** Indicate RD list end has not been reached when processing descriptors. (Set and Reset by HW)
0	-	RW	**RUN.** Enable queues to operate. (Set and Reset by SW)

Offest 37h ~ 36h: Rx Descriptor Control Register 0 Clear. (RDCSR.c)

Description: Write 1 will clear RDCSR bits and will not take effect if write 0

Bit	Default	Type	Description
15-8	0	R0	**Reserved**
7-4	0	RW0	**Bit definitions are the same as RDCSR0.s(0X32h)**

Offset 3Bh ~ 38h: Rx Descriptor Base Address Low Register . (RxDsBase.Lo)

Bit	Default	Type	Description
31-6	‘h0	RWU	**RxDsBase.Lo[31:6]**. RD base address Low
5-0	‘h0	R0	R/W as 0 always. For descriptor alignment issue

Offset 3Dh ~ 3Ch: Current Rx Descriptor Index Register (RDINDX)

Description: Current Receive Descriptor List Index maintained by HC in ring structure.

Bit	Default	Type	Description
15-0	‘h0	RU	**RdIndex**. Current indexed RD, will cross top while reach the RDCSIZE defined in 0x50h.

Offset 3Fh ~ 3Eh: Pending Timer For Tx Queue/Rx Queue Empty Interrupt (TQETMR, RQETMR)

Description: The unbalanced bandwidth between host side (PCI) and media side will induce the internal TXFIFO/RXFIFO to reach empty state and issue interrupt event frequently. To avoid this, 2 dedicated timers are provide to pend this interrupt caused of TXFIFO/RXFIFO empty state respectively.

Bit	Default	Type	Description
31-30	'h0	RW	**RQETMS1,RQETMS0 :** Timer resolution selection RQETMS1 / RQETMS0 / Description: 0 0 1 us; 0 1 4 us; 1 0 16 us; 1 1 64 us
29-24	'h0	RW	**RQETMR.** Pending Time Count
23-22	'h0	RW	**TQETMS1, TQETMS0 :** Timer resolution selection TQETMS1 / TQETMS0 / Description: 0 0 1 us; 0 1 4 us; 1 0 16 us; 1 1 64 us
21-16	'h0	RW	**TQETMR : Pending Time Count**

Offset 43h ~ 40h: Tx Descriptor 0 Base Address Low Register (TdBase0.Lo)

Bit	Default	Type	Description
31-6	'h0	RW	**TdBase0Lo[31:6].** TD #0 Base Address Low
5-0	'h0	R0	R/W as 0 always. For Desc alignment issue

Offset 47h ~ 44h: Tx Descriptor 1 Base Address Low Register (TdBase1.Lo)

Bit	Default	Type	Description
31-6	'h0	RW	**TdBase1Lo[31:6].** TD #1 Base Address Low
5-0	'h0	R0	R/W as 0 always. For Desc alignment issue

Offset 48h ~ 4Bh: Tx Descriptor 2 Base Address Low Register (TdBase2.Lo)

Bit	Default	Type	Description
31-6	'h0	RW	**TdBase0Lo[31:6].** TD #2 Base Address Low
5-0	'h0	R0	R/W as 0 always. For Desc alignment issue

Offset 4Fh ~ 4Ch: Tx Descriptor 3 Base Address Low Register (TdBase3.Lo)

Bit	Default	Type	Description
31-6	'h0	RW	**TdBase3Lo[31:6].** TD #3 Base Address Low
5-0	'h0	R0	R/W as 0 always. For Desc alignment issue

Offset 53h ~ 50h: Descriptor Size Register (TDCSIZE, RDCSIZE)

Bit	Default	Type	Description
31-16	'h0	RW	**TDCSIZE.** Tx Descriptor list length in each TD queue. Only the 12 LSB is available in VT6122. The 4 MSB are leaved for future extension.
15-0	'h0	RW	**RDCSIZE.** Rx Descriptor list length in each TD queue. Only the 8 LSB is available in VT6122. The 8 MSB are leaved for future extension.

Offset 57h ~ 54h: Current Tx Descriptor Index. 0 ,1 Register . (0x54~0x57h, TdIndxn)

Description: Current Transmit Descriptor List Index maintained by HC in ring structure

Bit	Default	Type	Description
31-16	'h0	RU	**TdIndex1**. Current indexed TD in queue #1. Cross top while reaching the TDCSIZE (0x52h/0x53h)
15-0	'h0	RU	**TdIndex0**. Current indexed TD in queue #0. Cross top while reaching the TDCSIZE (0x52h./0x53h)

Offset 5Bh ~ 58h: Current Tx Descriptor Index 2, 3 Register (TdIndxn)

Description: Current Transmit Descriptor List Index maintained by VT6122 in ring structure.

Bit	Default	Type	Description
31-16	'h0	RU	**TdIndex3**. Current indexed TD in queue #3. Cross top while reaching the TDCSIZE (0x52h/0x53h) .
15-0	'h0	RU	**TdIndex2**. Current indexed TD in queue #2. Cross top while reaching the TDCSIZE (0x52h/0x53h)

Offset 5Dh ~ 5Ch: Tx Programmable Pause Frame Timer Register (TXPUTM)

Bit	Default	Type	Description
15-0	'h0	RW	**TXPUTM[15:0].** Software programmed pause frame timer in transmitted pause frame

Offset 5Fh ~ 5Eh: Flow Control Rx Descriptor Residue Count Register (RBRDU)

Description: This register shows the number of available Rx descriptor dynamically. This value will be used to enable flow control mechanism by sending pause frame.

Bit	Default	Type	Description
15-0	'h0	RU	**RBRDU**. Rx Descriptor buffer residue counts. Only 8 LSBs available. The 8 MSBs will be leaved for future extension. While CR0.RXON=0; the written value will update the Rx Descriptor buffer residue. While CR0.RXON=1; the written value will be added into the original residue.

FIFO Test Registers (Offset 67h~ 60h/ 6Ah 6Bh)

Offset 67h ~ 60h: Reserved

Offset (Hex)	Byte 3	Byte 2	Byte 1	Byte 0
60	Reserved			
64	Reserved			

Offset 6Ah: Reserved

Offset 6Bh: Reserved

CAM Control Registers (Offset 69h~ 68h)

Offset 68h: CAM Address Register (CAMADR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	CAMEN	A0C1	CA5	CA4	CA3	CA2	CA1	CA0

Bit	Default	Type	Description
7	0	RW	**CAMEN.** Enable CAM Read/Write command.
6	0	RW	A0C1. Address-CAM/VLAN-ID-CAM selection bit Address-CAM selected while A0C1=0 VLAN-ID-CAM selected while A0C1=1.
5-0	'h0	RW	**CA[5:0].** A-CAM/V-CAM Address.

Offset 69h: CAM Command Register (CAMCR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	PS1	PS0	AITRPKT	AITR16	CAMRD	CAMWR		

Bit	Default	Type	Description
7-6	'b00	RW	**Page Select.** Register page select of MAR/VCAM/PCAM. **PS** **PS** **0x10 ~ 0x17** **0x20** **0xc0** 0 0 MAR port INTHOTMR ptn (0,1,2,3) 0 1 CAM Mask Port TSUPPTHR ptn (4,5,6,7) 1 0 CAM Data Port RSUPPTHR ptn (0,1,2,3) 1 1 MAR port INTHOTMR ptn (4,5,6,7)
5	0	RW	**AITRPKT.** Partition part of Address-CAM space for interesting packets filtering. Interesting packets are OS or protocol dependent packets with special patterns. Such packets will be negotiated in advance and programmed in Address-CAM. 802.1Q related filtering mechanism will be skipped on interesting packets. **0**: No Interesting packet segment defined. 1: With Interesting packet segment defined.
4	0	RW	**AITR16.** Interesting packet segment in A-CAM size option. Available only while AITRPKT is enabled (set to 1) **0**: 8 entries (cam_add 56 ~ 63) 1: 16 entries (cam_add 48 ~ 63)
3	0	RWC	**CAMRD**. CAM read command, auto cleared. Work only while CAMEN is enabled.
2	0	RWC	**CAMWR**. CAM write command, auto cleared. Work only while CAMEN is enabled.
1-0	0	RW	**Reserved**

MII Management Port Control Status Registers (Offset 73h ~ 6Ch)

Offset 6Ch: MII Management Port Configuration Register (MIICFG)

Description: MIICFG should locate at suspend domain

Bit Nbr	7	6	5	4	3	2	1	0
Func	MPO1	MPO0	MFDC	PHYAD4	PHYAD3	PHYAD2	PHYAD1	PHYAD0

Bit	Default	Type	Description
7-6	'h0	RW	**MPO1, MPO0x.** MII management polling interval, time unit = MDC clock cycle **MPO 1** / **MPO 0** / MDCs: 0 / 0 / 1024; 0 / 1 / 512; 1 / 0 / 128; 1 / 1 / 64
5	0	RW	**MFDC.** Accelerate MDC speed 0: MDC = normal 1: MDC = 4X accelerating
4-0	'h1	RO	**PHYAD[4:0]**. VT6122 fix internal PHYAD as 'h01

Offset 6Dh: MII Management Port Status Register (MIISR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	MIIDL							

Bit	Default	Type	Description
7	0	RO	**MIIDL.** Indicate not at the Software/Timer polling cycle
6-0	0	RW	**Reserved**

Offset 6Eh: PHY Status Register 0 (PHYSR0)dd

Bit Nbr	7	6	5	4	3	2	1	0
Func	PHYRST	LINKGD		FDPX	SPDG	SPD10	RXFLD	TXFLC

Bit	Default	Type	Description
7	0	RO	**PHYRST.** Show the PHY.Reg0.Bit15, RESET while PHYRST=1, all other bits are junk
6	0	RO	**LINKGD.** Show PHY.Reg1.Bit2, Link Status
5	0	-	**Reserved**
4	1	RO	**FDPX.** Full duplex mode, Pri-Res-Result. Priority Resolution Result.
3	1	RO	**SPDG.** PHY in Giga mode, Pri-Res-Result. Priority Resolution Result.
2	0	RO	**SPD10.** PHY in 10M mode, Pri-Res-Result. Priority Resolution Result.
1	0	RO	**RXFLC.** Rx flow control capability. Pri-Res-Result. Priority Resolution Result.
0	0	RO	**TXFLC.** Tx flow control capability. Pri-Res-Result. Priority Resolution Result.

Offset 70h: MII Management Command Register (MII_CR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	MAUTO	RCMD	WCMD	MDPM	MOUT	MDO	MDI	MDC

Bit	Default	Type	Description
7	0	RW	**MAUTO.** MII management port auto polling enable.
6	0	RWC	**RCMD.** MII management port embedded read command. Self-cleared while reading is completed. Available only while MAUTO=0 and MDPM=0.
5	0	RWC	**WCMD.** MII management port embedded write command. Self-cleared while programming is completed. Available only while MAUTO=0 and MDPM=0.
4	0	RW	**MDPM.** MII management port direct programming enable.
3	0	RW	**MOUT.** MDIO pin output enable control in Direct Programming mode.
2	0	RW	**MDO.** MDIO pin output data in Direct Programming mode
1	0	RW	**MDI.** MDIO pin input data in Direct Programming mode**.**
0	0	RW	**MDC.** MDC pin output data in Direct Programming mode**.**

Note.

MII Embedded Programming

<WCMD>

- **Write the offset address to 0x71.**
- **Write the programmed value to 0x72/0x73**
- **Program MIICR.WCMD.**
- **Wait MIICR.WCMD cleared. The programming sequences are completed.**

<RCMD>

- **Write the offset address to 0x71.**
- **Program MIICR.RCMD.**
- **Wait MIICR.RCMD cleared. The reading sequences are completed.**
- **Read 0x72/0x73 to get the value.**

Offset 71h: MII Embedded Read/Write Address Port Register (MII_ADR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	SWMPL			MAD4	MAD3	MAD2	MAD1	MAD0

Bit	Default	Type	Description
7	0	RWC	**SWMPL**. Initiate the priority resolution process. Self-cleared while all cycles are completed.
6	0	RW	**Reserved.**
5	0	RW	**Reserved.**
4-0	0	RW	**MAD[4:0]**. Target PHY Map register address for embedded read write process.

Offset 73h ~ 72h: MII Embedded Read/Write Data Port Register(MII_DAT)

access method.

Bit	Default	Type	Description
15-0	‘h0	RW	**MII_DATA.** MII PHY Management embedded Read/Write data port.

Software Timer Registers (Offset 77h ~ 74h)

Offset 75h ~ 74h: Software Single-shot Timer 0 Register (SFTMR0)

Operation.

a. Set resolution (GCR.TM0US) and program SFTMR0 register.
b. Set CR2.Timer0En=1.
c. SFTMR0 will be loaded and count down.
d. As timer expired, set timer0 interrupt (ISR2.TMR0I)
e. After write clear the ISR. TMR0I, SFTMR0 will be reloaded and count down again.
f. Clear CR2.Timer0EN will stop the behavior.

Bit	Default	Type	Description
0-15	'h0	RW	**SFTMR0.** Software programmable Timer with single shot. GCR.TM0US = 0 Resolution = 1.31ms GCR.TM0US = 1 Resolution = 1.28 us

Offset 77h ~ 76h: Software Periodic Timer 1 Register (SFTMR1)

Operation:

a. Set resolution (GCR.TM1US) and program SFTMR1 register.
b. Set CR2.Timer1En=1.
c. SFTMR1 will be loaded and count down.
d. As timer expired, set timer1 interrupt (ISR2.TMR1I)
e. SFTMR1 will be reloaded and count down again after timer expired interrupt is issued.
f. Clear CR2.Timer1EN will stop the behavior.

Bit	Default	Type	Description
0-15	'h0	RW	**SFTMR1.** Software programmable Timer with Periodic shot. GCR.TM1US = 0 Resolution = 1.31ms GCR.TM1US = 1 Resolution = 1.28 us

Chip Configuration Registers (Offset 7Fh ~ 78h)

Offset 78h: ..... Chip Configuration Register A (CFG_A)

Description: Configuration for LED and Pre-OS Wake On Lan function. The values can be loaded from EEPROM or programmed by software directly.

Bit Nbr	7	6	5	4	3	2	1	0
Func	Reserved	Reserved	PHYLEDS1	PHYLEDS0	PMHCTG	Reserved	ABSHDN	PACPI

Bit	Default	Type	Description
7-6	0	RWE	**Reserved**.
5-4	2'b00	RWE	**PHYLEDS1.** PHY LED function selection. **PHYLEDS0.** (See Table 16)
3	0	RWE	**PMHCTG**. Option to skip 802.1p TAG field while calculating the CRC value of incoming pattern-match packets. **0**: TAG field is always skipped. 1: TAG field is included.
2	0	RWE	**Reserved**
1	0	RWE	**ABSHDN.** Abnormal shut-down wake up function
0	0	RWE	**PACPI.** Pre_ACPI wake up function**.**

Offset 79h: .....Chip Configuration Register B(CFG_B)

Description: Configuration for MAC function. Load from EEPROM while power up, can be updated by software directly.

Bit Nbr	7	6	5	4	3	2	1	0
Func	GTCKOPT	Reserved	CRSEOPT					

Bit	Default	Type	Description
7	0	RWE	**GTCKOPT.** 0: GTXCLK will be exported while LinkDown 1: GTXCLK will not be exported while LinkDown ***GTXCLK behavior:*** Link on 10/100 BT: GTXCLK always be stopped. Link on 1000BT: (GTCKOPT==0) → always running (GTCKOPT==1) → Running while LinkOn, Stop while Linkdown.
6	0	RWE	**Reserved**
5	0	RWE	**CRSEOPT**. Giga mode slot time option on receive side. 0: 512 bytes 1: 500 bytes in GIGA mode
4-0	0	RWE	**Reserved**

Offset 7Ah: ..... Chip Configuration Register C(CFG_C)

Description: Configuration for BROM bus support.

Bit Nbr	7	6	5	4	3	2	1	0
Func	EELOAD							

Bit	Default	Type	Description
7	0	RWE	**EELOAD.** Enable EEPROM embedded and direct programming, always 0 after power on and loading
6	0	RWE	**Reserved**
5	0	RWE	**Reserved**
4	0	RWE	**Reserved**
3	0	RWE	**Reserved**
2-0	'h0	RWE	**Reserved**

Offset 7Bh: ..... Chip Configuration Register D (CFG_D)

Description: Configuration for PCI capabilities. Load from EEPROM at power up, can be updated by software while MCR1.DIAG = 1.

Bit Nbr	7	6	5	4	3	2	1	0
Func	IODIS		CFG DACEN					

Bit	Default	Type	Description
7	0	RWE	**IODIS.** Disable IO access mode. Only support Memory Map IO access**.**
6	0	RWE	**Reserved**
5	0	RWE	**CFGDACEN.** Enable 64-bit addressing by issuing DAC command.
4	0	RWE	**Reserved**
3	0	RWE	**Reserved**
2-0	0	RWE	**Reserved**

Offset 7Ch: ..... DMA Configuration Register 0 (DCF0)

Description: Configuration for DMA control capabilities**.** Load from EEPROM at power up, can be updated by software.

Bit Nbr	7	6	5	4	3	2	1	0
Func						DMAL2	DMAL1	DMAL0

Bit	Default	Type	Description
7-3	0	RWE	**Reserved**
2-0	0	RWE	**DMALEN[2:0].** TX/Rx FIFO DMA Burst Length Control.

DMALN[2:0]	Length (DW)	DMALN[2:0]	Length(DW)
000	8	100	128
001	16	101	256
010	32	110	SF
011	64	111	SF

Offset 7Dh ..... DMA Configuration Register 1 (DCF1)

Description: Configuration for DMA Control capabilities. Load from EEPROM at power up, can be updated by software.

Bit Nbr	7	6	5	4	3	2	1	0
Func	Reserved	Reserved	XMRL	PERDIS	MRDPL	MRWAIT	MWWAIT	LATMEN

Bit	Default	Type	Description
7-6	0	RWE	**Reserved.**
5	0	RWE	**XMRL.** Disable Memory_Read_Line command supporting
4	0	RWE	**PERR_DIS.** Disable data parity generation and checking
3	0	RWE	**MRDPL:** Replace Memory Read Line command with Memory Read Multiple. Availab only when XMRL = 0.
2	0	RWE	**MRWAIT.** Master read insert one wait state 2-2-2-2
1	0	RWE	**MWWAIT.** Master write insert one wait state 2-2-2-2
0	0	RWE	**LATMEN.** Latency timer effect enable

Offset 7Eh: MAC Receive Configuration Register 0 (MCFG0)

Description: Configuration for MAC receive control capabilities. Load from EEPROM at power up, can be updated by software.

Bit Nbr	7	6	5	4	3	2	1	0
Func	RXARB	Reserved	RFT1	RFT0	LOW THOPT	PQEN	RTGOPT	VIDFR

Bit	Default	Type	Description
7	0	RWE	**RXARB.** Arbitration priority selection, interleave to RX FIFO DMA after 32DW transactions while TX FIFO DMA is in progress.
6	0	RWE	**Reserved.**
5-4	0	RWE	**RFT[1:0].** Receive FIFO threshold control.
3	0	RWE	**LOWTHOPT.** RX FIFO low threshold control watermark option, **0:** 7 QW 1: 15 QW
2	0	RWE	**PQEN*** Enable 802.1p/ 802.1Q tagging function
1	0	RWE	**RTGOPT*** Option for receiving packet behavior
0	0	RWE	**VIDFR.** Filter out those incoming packet with VLAN_ID mis-matched.

RFT 1	RFT 0	Description
0	0	128 bytes
0	1	512 bytes
1	0	1024 bytes
1	1	SF

**Note*

PQEN	RTGOPT	Behavior
0	**0**	**tx: all packet untagged** **rx: both untagged/tagged packets(NOT extracting tag)**
0	**1**	**tx: all packet untagged** **rx: ONLY untagged packets.(NOT extracting tag)**
1	**0**	**tx: all packet tagged** **rx: both untagged/tagged packets** **(Extract tag from tagged packet)**
1	**1**	**tx: all packet tagged** **rx: ONLY tagged packets** **(Extract tag from tagged packets)**

Offset 7Fh: MAC Transmit Configuration Register 1 (MCFG1)

Description: Configuration for MAC transmit control capabilities. Load from EEPROM at power up, can be updated by software.

Bit Nbr	7	6	5	4	3	2	1	0
Func	TXARB	Reserved	Reserved	Reserved	TXQBK1	TXQBK0	TXQNBK	SNAPOPT

Bit	Default	Type	Description
7	0	RWE	**TXARB.** Arbitration priority selection, interleave to TX FIFO DMA after 32DW transactions, while RX FIFO DMA is in progress
6	0	RWE	**Reserved**
5-4	‘b00	RWE	**Reserved**
3-2	‘b00	RWE	**TXQBK[1:0]** Non blocking mode packet threshold control. **TXQBK1** / **TXQBK0** / Description 0 / 0 / 64 pkts 0 / 1 / 32 pkts 1 / 0 / 128 pkts 1 / 1 / 8 pkts
1	0	RWE	**TXQNOBK.** Priority transmit Non-blocking mode.
0	1	RWE	**SNAPOPT.** Control bit for tag insertion on Snap-frame. **1**: Tag inserted from 13th byte 0: Tag inserted after SNAP coded.(21th byte)

Offset 81h ~ 80h: Reserved

Offset 82h: Power Management Capability Shadow Register (PMCC)

Description: Load from EEPROM at power up, can be updated by software for diagnosis purpose when PMCCDIAG=1

Bit Nbr	7	6	5	4	3	2	1	0
Func	DSI	D2_Dis	D1_Dis	D3c_En	D3H_En	D2_En	D1_En	D0_En

Bit	Default	Type	Description
7	0	RE	**DSI.**
6	0	RE	**D2_Dis.** Disable D2 power state support.
5	0	RE	**D1_Dis.** Disable D1 power state support.
4	1	RE	**D3c_En.** D3 cold (D3Aux) power state capable, can inset PME#, while defined wake up event coming.
3	1	RE	**D3h_En.** D3 hot power state capable, can inset PME#, while defined wake up event coming.
2	1	RE	**D2_En.** D2 low power state capable, can inset PME#, while D2_Dis = 0, a defined wake up event coming.
1	1	RE	**D1_En.** D1 low power state capable, can inset PME#, while D1_Dis = 0, a defined wake up event coming.
0	0	RE	**D0_En.** D3 cold (D3Aux)power state capable, can inset PME#, while defined wake up event coming.

Offsest 83h: PMU Sticky Bit Shadow Register. (0x83h, STKSHDW)

Bit Nbr	7	6	5	4	3	2	1	0
Func							DS1	DS0

Bit	Default	Type	Description
7-5	0	RO	**Reserved.**
4	0	RW	**Reserved.**
3	0	RW0	**Reserved.**
2	0	RW	**Reserved.**
1-0	0	RW	**STKDS[1:0].** Sticky power state indicator in suspend well; software must maintain the power state consistency between suspend well and device state.

MIB Counter Control and Status Registers (Offset 84h, 8Bh ~ 88h)

Offset 84h: ..... MIB Counter Control and Status Register

Description:

Initialization
During chip initialization, MIBCR.MIBCLR should be toggled to clear all MIB counters.

Event Accumulation
32 8-bits temporary real-time counters are standby to count up 32 possible network events at the same time.

MIB SRAM Update
When any real-time counter reaches a pre-defined threshold, all those 32 8-bit counters will be flushed into MIB SRAM.

NearFull Warning
When any of MIB SRAM entries reaches a pre-define watermark, an interrupt will be issued (ISR2.MIBFI) to have a near full warning message. The Read-out action is required to avoid those MIB counters overflow

Host Read MIB (Hardware advance SRAM read pointer first and issue embed read)
1. Toggle MIBCR.MBTRINI, the 1st entry of MIB SRAM will be popped out and self-cleared. The value will be read from MIB_DAT port.
2. After reading the MIB_DAT port to get the 1st value, the 2nd entry of MIB SRAM will be popped and self-cleared automatically.
3. Iteratively reading MIB_DAT for 32 times can get all the MIB SRAM entries in sequence.
4. During the process that host reading MIB SRAM, all the network events are kept counted by real-time counter and MIB SRAM that guarantees no events missed.

MIB clear
Software can try to reset all MIB contents by toggling MIBCR.MIBCLR. During this period, those incoming events will be missed.

Bit Nbr	7	6	5	4	3	2	1	0
Func	MIBISTOK	MBISTGO		MIBHI	MIBFRZ	MIBFLSH	MPTRINI	MIBCLR

Bit	Default	Type	Description
7	0	RW0U	**MIBISTOK**. MIB Bist check status, write clear. 0: succeed 1: fail
6	0	RW	**MBISTGO**. Trigger MIB counter bist, work only while DIAG = 1;
5	0	RW	**Reserved**
4	0	RW	**MIBHI**. MIB counter near full on higher condition. 0: 24'h80_0000 1: 24'hc0_0000
3	0	RW	**MIBFREEZE**. Freeze MIB counter increment;
2	0	RW	**MIBFLUSH.** Force flush real time counts into MIB SRAM;
1	0	RW	**MBTRINI**. Return MIB read pointer to 0, and the MIB embedded logic will read the index-0 MIB counter value to MIB_DAT port. Read as 0 always.
0	0	RW	**MIBCLR.** Clear the MIB SRAM contents.

Offset 8Bh ~ 88h: MIB Counter Data and Address Output Port Registers (MIBDATA)

Description: VT6122 supports 32-sets 24 bit network event statistics counters for management.

Bit	Default	Type	Description
31-24	0	RO	**MIB_Ptr.** MIB counter index.
23-0	0	RO	**MIB_Data.** MIB counter value

Offset 85h: EE_SWDATA (0x85. EESWDAT)

Bit	Default	Type	Description
0-7	0	RO	8 bit EEPROM loaded data. leave for software usage.

Flash ROM Control Registers (Offset 91h ~ 8Ch)

Offset 8D ~ 8C: EEPROM Embedded Write Data Register

Bit	Default	Type	Description
15-0	'h0	RW	**EE_WRT_DAT**. EEPROM embedded write data port. Read data port at 0x94~0x95h

Offset 8E : Reserved

Offset 8F : Reserved

Offset 90h: Reserved

Offset 91h: Reserved

EEPROM Control Registers (Offset 97h ~ 92h)

Offset 92h: EPROM Checksum Field Shadow Register (EEChkSum)

Description: Shadow EEPROM CheckSum field here for reference

Bit	Default	Type	Description
7-0	-	RE	**EEChkSum.** EEPROM checksum fielder shadow.

Offset 93h: EEPROM Embedded Control and Status Register (EECSR)

Description: VT6122 supports 4-wire serial EEPROM like 93c06, 93c46. The embedded controller provides the capability.

Dynamic Reload :Reload all EEPROM content.
Embedded read or write EEPROM in word basis
Direct Programming read write EEPROM for manufacturing purpose

Bit Nbr	7	6	5	4	3	2	1	0
Func	Reserved	EMBP	RELOAD	DPM	ECS	ECK	EDI	EDO

Bit	Default	Type	Description
7	0	RO	**Reserved.**
6	0	RW	**EMBP.** EEPROM Embedded Program mode enable. Programmable only when CFGC.EELOAD=1.
5	0	RWC	**RELOAD.** Dynamic reload EEPROM
4	0	RW	**DPM. EEPROM** Direct Program mode enable.
3	0	RW	**ECS.** EEPROM interface CS output on direct-program mode
2	0	RW	**ECK.** EEPROM interface CK output on direct-program mode
1	0	RW	**EDI.** EEPROM interface DI output on direct-program mode
0	-	RO	**EDO.** EEPROM interface DO status on direct-program mode

Offset 95h ~ 94h: EEPROM Embedded Read Data Port Register (EE_RD_DATA)

Bit	Default	Type	Description
15-0	'h0	RW	**EE_RD_DATA.** EEPROM Embedded Read data port.

Offset 96h: EEPROM Embedded Read Address Port Register (EADDR)

Description: 93c06/93c46 are supported in VT6122

Bit	Default	Type	Description
0-7	'h0	RW	**EEADDR[7:0].** EEPROM Embedded operation address port

Offset 97h: EEPROM Embedded Control and Status Register (EMCMD)

Bit Nbr	7	6	5	4	3	2	1	0
Func	EDONE				EWDIS	EWEN	EWR	ERD

Bit	Default	Type	Description
7	1	RU	**EDONE**. Embedded read/write done 0: EMBEEWDI|EMBEEWEN|EMBEERD are set **1:** Embedded command(s) finished
6-4	0	RW	**Reserved.**
3	0	RWC	**EWDIS**. Embedded program EEPROM into write disable mode; self-cleared while finished.
2	'h0	RWC	**EWEN.** Embedded program EEPROM into write enable mode; self-cleared while finished.
1	0	RWC	**EWR.** Embedded write EEPROM with pre-defined address and data. self-cleared while finished.
0	0	RWC	**ERD.** Embedded read EEPROM with pre-defined address; self-cleared while finished.

Note: **EEPROM write operation must follow the sequence:**

EEWEN → EEWR → EEWR ……. → EEWDIS

Jumper Strapping Status Registers (Offset 9Bh~ 98h)

Offset 98h: Reserved

Offset 99h: Chip Jumper Strapping status Register (CJMPSR)

Access Type: Jumper strapping status related to chip function

Bit Nbr	7	6	5	4	3	2	1	0
Func		XIBYPS (LED3)	EEDIS (ECS)				TSTM1	TSTM0

Offset 9Ah: Reserved

Offset 9Bh: Media Jumper Strapping status Register 3 (MJMPSR)

Bit Nbr	7	6	5	4	3	2	1	0
Func			VEESEL					

Offset 9Ch: Chip Operation and Diagnosis Status Register (CHIPGSR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	DLL INPHAS		POR	EEPR			PCI SPD66	PMU10

Bit	Default	Type	Description
7	0	RO	**DLLINPHASE.** DLL in-phase status.
6	0	RO	
5	0	RO	**POR**. Power on reset generator self test status
4	0	RO	**EEPR.** EEPROM load complete indication during power up sequence and 73h is detected.
3	0	RO	**Reserved**
2	0	RO	**Reserved**
1	0	RO	**PCISPD66**. Indicate PCI running in 66Mhz.
0	0	RO	**PMU10.** PMC supports version. EEPROM loaded status.

Offset 9Dh: Reserved

Offset 9Eh: ..... Chip Debug Control Register (DEBUG)

Bit Nbr	7	6	5	4	3	2	1	0
Func				PMCC DIAG	FPSTIME	ACPFRM		

Bit	Default	Type	Description
7	0	RW	**Reserved.**
6	0	R0W	**Reserved.**
5	0	RW	**Reserved.**
4	0	RW	**PMCDIAG.** PMCC (0x82h) setting test mode can be R/W while PMCCDIAG=1
3	0	RW	**FPSTIME.** Force received pause frame timer **0**: The pause timer follows received pause frame pause_timer. 1: The pause timer is forced to 16'h0010;
2	0	RW	**ACPFRM.** Accept pause frame to system buffer.
1	0	RW	**Reserved**
0	0	RW	**Reserved**

Offset 9Fh: Chip Operation and Diagnosis Control Register (CHIPGCR)

Bit Nbr	7	6	5	4	3	2	1	0
Func	FCGMII	FCFDX	FCRESV	FCMODE	LPSOPT	TM1US	TM0US	PHYINTEN

Bit	Default	Type	Description
7	0	RW	**FCGMII.** While FCMODE =1, software forces MAC operating on GMII mode, else operating in MII mode.
6	0	RW	**FCFDX.** Software forces MAC operating on Full Duplex mode. Available only when FCMODE = 1.
5	0	RW	**FCRESV.** Reserved for future Fiber mode usage
4	0	RW	**FCMODE**. Program MAC side into force mode
3	0	RW	**LPSOPT.** Option to disable LPSEL field in priority resolution.
2	0	RW	**TM1US**. Software Timer 0 in micro-second resolution.
1	0	RW	**TM0US**. Software Timer 0 in micro-second resolution.
0	0	RW	**PHYINTEN.** Enable PHY interrupt passed through INTA_. Available only when CFGA.GPIO1PD are set to 0.

Wake On Lan Registers

Offset A0h: Wake On Lan Event Enable Set Register (WOLCR0.s)

Offset A4h: Wake On Lan Event Enable Control Register (WOLCR0.c)

Description: For set port, write 1 means Set to 1, write 0 has no effect
For clear port, write 1 means Clear to 0, write 0 has no effect, read value is as same as Set port.

Bit Nbr	7	6	5	4	3	2	1	0
Func	PTNMH7	PTNMH6	PTNMH5	PTNMH4	PTNMH3	PTNMH2	PTNMH1	PTNMH0

Bit	Default	Type	Description
7	0	RW1	**PTNMH7.** Enable WOL event detection of Patten Match, pattern #7
6	0	RW1	**PTNMH6.** Enable WOL event detection of Patten Match, pattern #6**.**
5	0	RW1	**PTNMH5.** Enable WOL event detection of Patten Match, pattern #5
4	0	RW1	**PTNMH4.** Enable WOL event detection of Patten Match, pattern #4
3	0	RW1	**PTNMH3.** Enable WOL event detection of Patten Match, pattern #3
2	0	RW1	**PTNMH2.** Enable WOL event detection of Patten Match, pattern #2
1	0	RW1	**PTNMH1.** Enable WOL event detection of Patten Match, pattern #1
0	0	RW1	**PTNMH0.** Enable WOL event detection of Patten Match, pattern #0

Offset A1h: Wake On Lan Event Enable Set Register (WOLCR1.s)

Offset A5h: Wake On Lan Event Enable Control Register. (WOLCR1.c)

Bit Nbr	7	6	5	4	3	2	1	0
Func					LinkOff En	LinkOn En	MAGICEN	UNIQEN

Bit	Default	Type	Description
7	0	RW1	**Reserved**
6	0	RW1	**Reserved**
5	0	RW1	**Reserved**
4	0	RW1	**Reserved**
3	0	RW1	**LinkOffEn**. Enable WOL event detection for link On to Link Fail
2	0	RW1	**LinkOnEn**. Enable WOL event detection for link Fail to Link On.
1	0	RW1	**MagicEn**. Enable WOL event detection for Magic Packet.
0	0	RW1	**UniQEN**. Enable WOL event detection for receiving an unicast packet with recognized Ethernet address

Offset A2h: Power Management Configuration Set Register (PWCFG.s)

Offset A6h: Power Management Configuration Control Register (PWCFG.c)

Description: Internal updated by hardware control for Wake-On-Lan events are detected.
Write 1 means set for testing purpose. Write 0 has no effect

Bit Nbr	7	6	5	4	3	2	1	0
Func					PME_SR	PME_EN		

Bit	Default	Type	Description
7	0	RW1S	**Reserved**
6	0	RW1S	**Reserved**
5	0		
4	0		
3	0	RW1S	**PME_SR.** PMCSR PME_SR shadow, testing purpose
2	0	RW1S	**PME_EN.** PMCSR, PME_EN shadow
1	0		
0	0		

Offset A3h: Wake-On-Lan Configuration Set Register (WOLCFG.s)

Offset A7h: Wake-On-Lan Configuration Control Register (WOLCFG.c)

Description:

1. All filtering results will be qualified with RXOKEOF. In WOL mode, PROM=0, SEP=0, AR=0, RXOKEOF = normal_accept in AB=1, AM=1 & accept Physical packet
2. Whenever power status is set, the receiver will be blocked until software interleave to turn on the receiver again.
3. When entering WOL detected state receiver, packet acceptation is controlled by SAB /SAM/RXOKEOF

Bit Nbr	7	6	5	4	3	2	1	0
Func			SAM	SAB				PHY EVTEN

Bit	Default	Type	Description
7	0	RW1S	**Reserved**.
6	0	RW1S	**Reserved**
5	0	RW1	**SAM.** Accept multicast packet in power mode**.**
4	0	RW1S	**SAB.** Accept broadcast packet in power mode.
3	0	RW1S	**Reserved**
2	0	RW1S	**Reserved**
1	0	RW1S	**Reserved**
0	0	RW1S	**PHYEVTEN.** Using PHYINT as status change report Available only while CFGA.GPIO1PD are set to 0

Offset A8h: Wake On Lan Event Status Set Register (WOLSR0.s)

Offset ACh: Wake On Lan Event Status Control Register (WOLSR0.c)

Description: Internal updated by hardware control for Wake On Lan events are detected
Write 1 means set for testing purpose. Write 0 has no effect

Bit Nbr	7	6	5	4	3	2	1	0
Func	PTNMH7I	PTNMH6I	PTNMH5I	PTNMH4I	PTNMH3I	PTNMH2I	PTNMH1I	PTNMH0I

Bit	Default	Type	Description
7	0	RW1S	**PTNMH7Int.** WOL event detected of Patten Match, pattern #7
6	0	RW1S	**PTNMH6Int.** WOL event detected of Patten Match, pattern #6
5	0	RW1S	**PTNMH5Int.** WOL event detected of Patten Match, pattern #5
4	0	RW1S	**PTNMH4Int.** WOL event detected of Patten Match, pattern #4
3	0	RW1S	**PTNMH3Int.** WOL event detected of Patten Match, pattern #3
2	0	RW1S	**PTNMH2Int.** WOL event detected of Patten Match, pattern #2
2	0	RW1S	**PTNMH1Int.** WOL event detected of Patten Match, pattern #1
1	0	RW1S	**PTNMH0Int.** WOL event detected of Patten Match, pattern #0
0	0	RW1S	**PTNMH7Int.** WOL event detected of Patten Match, pattern #7

Offset A9h: Wake On Lan Event Status Set Register. (0xA9h, WOLSR1.s)

Offset ADh: Wake On Lan Event Status Control Register. (0xADh, WOLSR1.c)

Bit Nbr	7	6	5	4	3	2	1	0
Func					LinkOffI	LinkOnI	MAGCENI	UNIQENI

Bit	Default	Type	Description
7	0	RW1S	**Reserved.**
6	0	RW1S	**Reserved.**
5	0	RW1S	**Reserved.**
4	0	RW1S	**Reserved.**
3	0	RW1S	**LinkOffI.** WOL event detected while link status changed from link On to Link Off
2	0	RW1S	**LinkOnI.** WOL event detected while link status changed from link Off to Link On.
1	0	RW1S	**MAGCENI.** WOL event detected while Magic Packet received.
0	0	RW1S	**UNIQENI.** WOL event detected while an unicast packet received.

Offset BFh ~ B0h: 8 Groups of 16-bits CRC Register (PTNCRC)

Description: Those CRC value are all pre-defined for pattern match packet Wakeup usage.

Offset B3h ~ B0h

Bit	Default	Type	Description
31:16	0	RW	**Pattern Match group 1 CRC16 value**
15:0	0	RW	**Pattern Match group 0 CRC16 value**

Offset B7h ~ B4h

Bit	Default	Type	Description
31:16	0	RW	**Pattern Match group 3 CRC16 value**
15:0	0	RW	**Pattern Match group 2 CRC16 value**

Offset BBh ~ B8h

Bit	Default	Type	Description
31:16	0	RW	**Pattern Match group 5 CRC16 value**
15:0	0	RW	**Pattern Match group 4 CRC16 value**

Offset BFh ~ BCh

Bit	Default	Type	Description
31:16	0	RW	**Pattern Match group 7 CRC16 value**
15:0	0	RW	**Pattern Match group 6 CRC16 value**

Offset FFh ~ C0h: 8 Groups of 128 bit Pattern Match Bit Mask Register (PTNBMSK)

Description: Those bit masks value are all pre-defined for pattern match packet Wakeup usage. Two pages selected by {CAMCR.PS0, CAMCR.PS1}

Offset CF ~ C0h

Bit	Default	Type	Description
31:0	0	RW	**Pattern Match group 0/4 bit mask [127:96]**
31:0	0	RW	**Pattern Match group 0/4 bit mask [95:64]**
31:0	0	RW	**Pattern Match group 0/4 bit mask [63:32]**
31:0	0	RW	**Pattern Match group 0/4 bit mask [31:0]**

Offset DF ~ D0h

Bit	Default	Type	Description
31:0	0	RW	**Pattern Match group 1/5 bit mask [127:96]**
31:0	0	RW	**Pattern Match group 1/5 bit mask [95:64]**
31:0	0	RW	**Pattern Match group 1/5 bit mask [63:32]**
31:0	0	RW	**Pattern Match group 1/5 bit mask [31:0]**

Offset EF ~ E0h

Bit	Default	Type	Description
31:0	0	RW	**Pattern Match group 2/6 bit mask [127:96]**
31:0	0	RW	**Pattern Match group 2/6 bit mask [95:64]**
31:0	0	RW	**Pattern Match group 2/6 bit mask [63:32]**
31:0	0	RW	**Pattern Match group 2/6 bit mask [31:0]**

Offset FF ~ F0h

Bit	Default	Type	Description
31:0	0	RW	**Pattern Match group 3/7 bit mask [127:96]**
31:0	0	RW	**Pattern Match group 3/7 bit mask [95:64]**
31:0	0	RW	**Pattern Match group 3/7 bit mask [63:32]**
31:0	0	RW	**Pattern Match group 3/7 bit mask [31:0]**

MII Registers

The MII register bit modes are defined in the following table.

Access Type	Description	Access Type	Description
R/W	Read and Write	**R/O**	Read Only
LH	Latched High	**LL**	Latched Low
SC	Self-Cleared	**RS**	Reset-Sticky

Register conventions are as follows:

- "Reset value" refers to the state of register bit(s) after *either* a hardware *or* a software reset. The only difference between a hardware and software reset is that all internal analog reference voltages and currents, including the PLL, are powered down while a hardware reset is asserted, but are not powered down while a software reset is asserted.
- "Reset-Sticky" refers to register bit(s) that may not be reset when a software reset is issued.

Offset 00h: Mode Control Register

Bit	Default	Type	Description
15	0	R/W SC	**Software Reset.** Software reset (i.e. setting Software Reset to "1") is self-clearing (i.e. automatically set to "0"). The only difference between the hardware and software reset is that the hardware reset also powers down all internal analog reference voltages and currents, including the PLL. Once Software Reset is asserted, the integrated PHY is returned to normal operating mode and is ready for the next MII transaction, so Software Reset always reads back "0". Software Reset restores all MII registers to their default states unless the reset-sticky control bit 28.1 is set. When control bit 28.1 is set to "1", the reset-sticky bits retain their values after a software reset.. 1 = Reset asserted **0** = Reset de-asserted
14	0	R/W	**Loopback.** When Loopback is asserted, the Transmit Data (TXD) coming from the integrated MAC interface is looped back as Receive Data (RXD) to the integrated PHY. In loopback mode, no signal is transmitted over the network media. The loopback mechanism works in all (10/100/1000) modes of operation. The operating mode is determined by MII register bits, 0.6, 0.13 (Forced Speed Selection) 1 = Loopback on **0** = Loopback off
6, 13	See note below	R/W	**Forced Speed Selection.** These bits determine the 10/100/1000 speed when Auto-Negotiation is disabled by clearing MII bit 0.12. These bits are ignored if bit 0.12 is set. Note that Auto-Negotiation is always required in 1000BASE-T mode in normal operating modes. These bits also set the operating mode when loopback (0.14) is set to "1". 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved
12	1	R/W	**Auto-Negotiation Enable.** After a power-up or reset, the integrated PHY automatically activates the Auto-Negotiation state machine, setting bit 12 to "1". If bit 12 is written to a "0", the Auto-Negotiation process is disabled, and the present contents of the PHY's MII register bits determine the operating characteristics. Note that Auto-Negotiation is always required in 1000BASE-T mode. 1 = Auto-Negotiation on 0 = Auto-Negotiation off
11	0	R/W	**Power-Down.** Power-Down functions the same as Software Reset, except that it is not self-clearing, and that R/W MII bits are not restored to their default states by Power-Down. After Power-Down is deactivated (i.e., set to "0"), the PHY will be ready for normal operation before the next SMI transaction. If Auto-Negotiation is enabled, the PHY will begin Auto-Negotiation immediately upon exiting Power-Down. 1 = Power-down **0** = Power-up
10	0	R/W	**Reserved**
9	0	R/W SC	**Restart Auto-Negotiation.** When Restart Auto-Negotiation is asserted (i.e., set to "1"), the Auto-Negotiation state machine will restart the Auto-Negotiation process, even if it is in the middle of an Auto-Negotiation process. This control bit is self-clearing, and will always return a "0" when read. 1 = Restart MII 0 = Normal operation
8	1	R/W	**Duplex Mode**. The VT6122operates in half-duplex by default when auto-negotiation is disabled. The VT6122 can be reconfigured to operate in full-duplex by setting the Duplex Mode bit to "1" while Auto-Negotiation is disabled by clearing bit 0.12. Changes to the state of Duplex Mode while Auto-Negotiatio is enabled are ignored. 1 = Full duplex 0 = Half duplex

Bit	Default	Type	Description
7	0	R/W	**Collision Test Enable.** The collision test mode allows the COL pins to be tested during loopback mode. While the collision test mode is enabled (by setting Collision Test Enable to a "1"), asserting TX_EN will cause the COL output to go high within 512 bit times. De-asserting TX_EN will cause the COL output to go low within 4 bit times. The collision test mode should be enabled only when loopback is enabled. 1 = Collision test enabled **0** = Collision test disabled
6	1	-	See bit 0.13
5:0	0	-	**Reserved**

Offset 01h: Mode Status Register

Bit	Default	Type	Description
15	0	RO	**100BASE-T4 Capability** The VT6122 is not 100BASE-T4 capable, so this bit is hard-wired to "0". 1 = 100BASE-T4 capable
14	1	RO	**100BASE-X FDX Capability** The VT6122 is 100BASE-X FDX capable, so this bit is hard-wired to "1". 1 = 100BASE-X FDX capable
13	1	RO	**100BASE-X HDX Capability** The VT6122 is 100BASE-X HDX capable, so this bit is hard-wired to "1". 1 = 100BASE-X HDX capable
12	1	RO	**10BASE-T FDX Capability** The VT6122 is 10BASE-T FDX capable, so this bit is hard-wired to "1". 1 = 10BASE-T FDX capable
11	1	RO	**10BASE-T HDX Capability** The VT6122 is 10BASE-T HDX capable, so this bit is hard-wired to "1". 1 = 10BASE-T HDX capable
10	0	RO	**100BASE-T2 FDX Capability** The VT6122 is not 100BASE-T2 FDX capable, so this bit is hard-wired to "0". 1 = 100BASE-T2 FDX capable
9	0	RO	**100BASE-T2 HDX Capability** The VT6122 is not 100BASE-T2 HDX capable, so this bit is hard-wired to "0". 1 = 100BASE-T2 HDX capable
8	1	RO	**Extended Status Enable** The VT6122 is extended status capable, so this bit is hard-wired to "1". 1 = Extended status information present in Register 15
7	0	RO	**Reserved**
6	1	RO	**Preamble Suppression Capability.** This bit is hard-wired to 1. **1** = Mgmt Frame preamble may be suppressed 0 = Mgmt Frame preamble always required
5	0	RO	**Auto-Negotiation Complete.** When this bit is "1", the contents of Registers 4, 5, 6, and 15 are valid. 1 = Auto-Negotiation complete **0** = Auto-Negotiation not complete
4	0	RO LH	**Remote Fault.** Bit 1.4 will be set to "1" if the Link Partner signals a far-end fault. The bit is cleared automatically upon a read if the far-end fault condition has been removed. 1 = Far-end fault detected **0** = No fault detected
3	1	RO	**Auto-Negotiation Capability.** The VT6122 is Auto-Negotiation capable, so this bit is hard-wired to "1". Note that this bit will read "1" even if Auto-Negotiation is disabled via bit 0.12. 1 = Auto-Negotiation capable
2	0	RO LL	**Link Status.** This bit will return to "1" when the VT6122 link state machine has reached the "link pass" state, meaning that a valid link has been established. If the link is subsequently lost, the Link Status will revert to "0" state. It will remain "0" until Link Status is read while the link state machine is in the "link pass" state. In this case, Link Status will return to "0", but it will return "1" on subsequent reads as long as the "link pass" state is maintained. 1 = Link is up (Link pass) 0 = Link is down (Link fail)
1	0	RO LH	**Jabber Detect**. Note that Jabber Detect is required for 10BASE-T mode only. Jabber Detect will be set to "1" when the jabber condition is detected. Jabber Detect will be cleared automatically when this register is read. 1 = Jabber condition detected 0 = No jabber condition detected
0	1	RO	**Extended Capability.** The VT6122 has extended register capability, so this bit is hard-wired to "1". 1 = Extended register capable

Offset 02h: PHY Identifier Register #1

Bit	Default	Type	Description
15:0	000Fh	RO	**Organizationally Unique Identifier**. OUI least significant bits Per IEEE requirements, only OUI bits 3 to 18 are used in this register.

Offset 03h: PHY Identifier Register #2

Bit	Default	Type	Description
15:10	31h	RO	**Organizationally Unique Identifier**. OUI most significant bits Per IEEE requirements, only OUI bits 19 to 24 are used in this register.
9:4	20h (64-bit) or 21h (32-bit)	RO	Vendor Model Number (IC).
3:0	1h	RO	Vendor Revision Number (IC).

Offset 04h: Auto-Negotiation Advertisement Register

Description: This register controls the advertised abilities of the local (not remote) PHY. The state of this register is latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Thus, any writes to this register prior to completion of Auto-Negotiation as indicated by bit 1.5 should be followed by a re-negotiation for the new values to be properly used for Auto-Negotiation. Once Auto-Negotiation has completed, this register value may be read via the SMI to determine the highest common denominator technology.

Bit	Default	Type	Description
15	0	R/W	**Next-Page Transmission Request**. In 1000BASE-T, there are required Next-Pages transmitted per the standard. The user may optionally transmit additional Next-Pages. The VT6122 supports additional Next-Page transmission. Bit 4.15 is set by the user to request additional Next-Page transmission. See description of register 18.1 for more details on Next-Page exchanges. 1 = Next-Page transmission request
14	0	RO	**Reserved**
13	0	R/W	**Transmit Remote Fault.** The state of this bit is transmitted to the Link Partner during Auto-Negotiation. This bit does not have any effect on the local PHY operation. This bit is automatically cleared following a successful negotiation with the Link Partner. 1 = Transmit remote fault
12	0	R/W	**Reserved technologies.**
11	1	R/W	**Advertise Asymmetric Pause.** This bit is used by the local MAC to communicate pause capability to the Link Partner; it has no effect on PHY operation. 1 = Advertise Asymmetric Pause capable
10	1	R/W	**Advertise Symmetric Pause.** This bit is used by the local MAC to communicate pause capability to the Link Partner; it has no effect on PHY operation. 1 = Advertise Symmetric Pause capable
9	0	R/W	**Advertise 100BASE-T4 Capability.** Bits [9:5] allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the local PHY. By writing "1" to any of the bits, the corresponding ability will be advertised to the Link Partner. Writing "0" to any bit causes the corresponding ability to be suppressed from transmission. The state of these bits has no other effect on the operation of the local PHY. Resetting the chip restores the default bit values. Note that the default values of these bits indicate the true ability of the VT6122. 1 = 100BASE-T4 capable
8	1	R/W	**Advertise 100BASE-X FDX.** (See Bit 9 for detailed description) 1 = 100BASE-X FDX capable
7	1	R/W	**Advertise 100BASE-X HDX.** (See Bit 9 for detailed description) 1 = 100BASE-X HDX capable
6	1	R/W	**Advertise 10BASE-T FDX.** (See Bit 9 for detailed description) 1 = 10BASE-T FDX capable
5	1	R/W	**Advertise 10BASE-T HDX.** (See Bit 9 for detailed description) 1 = 10BASE-T HDX capable
4:0	01h	R/W	**Advertise Selector Field.** Since the VT6122 is a member of the 802.3 class of PHYs, the Advertise Selector Field defaults to "00001". These bits are R/W only because the Ethernet standard requires them to be R/W. However, these bits should not be changed because an 802.3 PHY uses them to verify that the Link Partner is also an 802.3 PHY before completing Auto-Negotiation.

Offset 05h: Auto-Negotiation Link Partner Ability Register

Bit	Default	Type	Description
15	0	RO	**LP Next-Page Transmit Request.** This bit returns "1" when the Link Partner implements the Next-Page function and has Next-Page information it wants to transmit. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set. 1 = LP NP transmit request
14	0	RO	**LP Acknowledge.** This bit returns "1" when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3. 1 = LP acknowledge
13	0	RO	**LP Remote Fault.** This bit returns "1" when the Link Partner signals that a remote fault (from its perspective) has occurred. The local PHY does not otherwise use this bit. 1 = LP remote fault
12	0	RO	**Reserved technologies**
11	0	RO	**LP Asymmetric Pause Capability**. The LP Asymmetric Pause Capability bit indicates whether the Link Partner has asymmetric pause capability. This bit is used by the Link Partner's MAC to communicate symmetric pause capability with the local MAC; it has no effect on PHY operation. 1 = LP Asymmetric Pause capable
10	0	RO	**LP Symmetric Pause Capability**. The LP Symmetric Pause Capability bit indicates whether the Link Partner supports symmetric pause frame capability. This bit is used by the Link Partner's MAC to communicate symmetric pause capability to the local MAC; it has no effect on PHY operation. 1 = LP Symmetric Pause capable
9	0	RO	**LP Advertise 100BASE-T4 Capability**. Bits [9:5] reflect the abilities of the Link Partner. The value "1" on any one of these bits indicates that the Link Partner advertises capability of performing the corresponding mode of operation. 1 = LP Advertise 100BASE-T4 capable
8	0	RO	**LP Advertise 100BASE-X FDX.** 1 = LP 100BASE-X FDX capable
7	0	RO	**LP Advertise 100BASE-X HDX**. 1 = LP 100BASE-X HDX capable
6	0	RO	**LP Advertise 10BASE-T FDX**. 1 = LP 10BASE-T FDX capable
5	0	RO	**LP Advertise 10BASE-T HDX**. 1 = LP 10BASE-T HDX capable
4:0	0	RO	**LP Advertise Selector Field**. Bits [4:0] indicate the state of the Link Partner's Selector Field. The local PHY does not otherwise use these bits.

Offset 06h: Auto-Negotiation Expansion Register

Bit	Default	Type	Description
15:5	0	RO	**Reserved**
4	0	RO LH	**Parallel Detection Fault.** Parallel Detection Fault returns "1" when a parallel detection fault occurs in the local Auto-Negotiation state machine. Once set, this bit is automatically cleared when (and only when) Register 6 is read. 1 = Parallel detection fault
3	0	RO	**LP Next-Page Able.** LP Next-Page Able returns "1" when the Link Partner has Next-Page capabilities. This bit is used in the Auto-Negotiation state machines, as defined in Clause 28 of IEEE 802.3. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set. 1 = LP Next-Page capable
2	1	RO	**Local PHY Next-Page Able.** Since the VT6122 is Next-Page able, this bit is hard-wired to "1". 1 = Next-Page capable
1	0	RO LH	**Page Received.** Page Received is set to "1" when a new Link Code Word is received from the Link Partner, validated, and acknowledged. Page Received is automatically cleared when (and only when) Register 6 is read. 1 = New page has been received
0	0	RO	**LP Auto-Negotiation Able.** LP Auto-Negotiation Capable is set to "1" if the Link Partner advertises Auto-Negotiation capability. The state of this bit is valid when the Auto-Negotiation Complete bit (1.5) or the Page Received bit (6.1) is set. 1 = LP Auto-Negotiation capable

Offset 07h: Auto-Negotiation Next-Page Transmit Register

Bit	Default	Type	Description
15	0	R/W	**Next Page**. The Next Page bit indicates whether this is the last Next-Page to be transmitted. By default, this bit is set to "0", indicating that this is the last page. 1 = More pages follow **0** = Last page
14	0	RO	**Reserved**
13	1	R/W	**Message Page**. The Message Page bit indicates whether this page is a message page or an unformatted page. This bit does not otherwise affect the operation of the local PHY. By default, this bit is set to "1", indicating that this is a message page. **1** = Message page 0 = Unformatted page
12	0	R/W	**Acknowledge2**. The Acknowledge2 bit indicates if the local MAC reports that it is able to act on the information (or perform the task) indicated in the previous message. The local PHY does not interpret or act on changes in the state of this bit. 1 = Will comply with request **0** = Cannot comply with request
11	0	RO	**Toggle**. The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. The Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word. 1 = Previous transmitted LCW == 0 **0** = Previous transmitted LCW == 1
10:0	01h	R/W	**Message/Unformatted Code**. The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner. The local PHY passes the message code to the Link Partner without interpreting or reacting to it. By default, this code is set to "000 0000 0001", indicating a null message.

Offset 08h: Auto-Negotiation Link Partner Next-Page Receive Register

Description: Register 8 contains the Link Partner's Next-Page register contents. The contents of this register are valid only when the Page Received bit (6.1) is set.

Bit	Default	Type	Description
15	0	RO	**LP Next Page.** This bit indicates if more pages follow from the Link Partner. 1 = More pages follow 0 = Last page
14	0	RO	**LP Acknowledge.** This bit returns "1" when the Link Partner signals that it has received the Link Code Word from the local PHY. The local PHY uses this bit for proper Link Code Word exchange, as defined in Clause 28 of IEEE 802.3. 1 = LP acknowledge
13	0	RO	**LP Message Page**. The Message Page bit indicates if the page received from the Link Partner is a message page or an unformatted page. 1 = Message page 0 = Unformatted page
12	0	RO	**LP Acknowledge2**. The Acknowledge2 bit indicates whether the Link Partner reports that it is able to act on the information (or perform the task) indicated in the message. The local PHY does not interpret or act on changes in the state of this bit. 1 = LP will comply with request
11	0	RO	**LP Toggle**. The Toggle bit is used by the arbitration function in the local PHY to ensure synchronization with the Link Partner during Next-Page exchanges. In the Link Partner, the Toggle bit is automatically set to the opposite state of the Toggle bit in the previously exchanged Link Code Word from the Link Partner. 1 = Previous transmitted LCW == 0 0 = Previous transmitted LCW == 1
10:0	0	RO	**LP Message/Unformatted Code**. The Message/Unformatted Code bits indicate the message code being transmitted to the Link Partner.

Offset 09h: 1000BASE-T Control Register

Bit	Default	Type	Description
15:13	0	R/W	**Transmitter Test Mode.** This test is valid only in 1000BASE-T mode. Refer to IEEE 802.3-2002, section 40.6.1.1.2 for more information. Described below, per IEEE 802.3-2002, 40.6.1.1.2. Use section Transmitter/Receiver Test Mode for reference
12	0	R/W	**MASTER/SLAVE Manual Configuration Enable**. When this bit is set to "0" (default), the MASTER/SLAVE designation of the local PHY is determined using the arbitration protocol established in the IEEE Ethernet standard. When this bit is set to "1", the MASTER/SLAVE designation of the local PHY is set by bit 9.11. Note that MASTER/SLAVE timing is valid only in 1000BASE-T mode. 1 = Enable MASTER/SLAVE Manual Configuration value **0** = Disable MASTER/SLAVE Manual Configuration value
11	0	R/W	**MASTER/SLAVE Manual Configuration Value**. This bit is ignored when bit 9.12 is set to "0". However, if bit 9.12 is set to "1", bit 9.11 determines the MASTER/SLAVE designation of the local PHY. If bit 9.12 is set to "1" and bit 9.11 set to "0" (default), the local PHY is forced to be a SLAVE. If bit 9.12 is set to "1" and bit 9.11 set to "1", the local PHY is forced to be a MASTER. Note that MASTER/SLAVE timing is valid only in 1000BASE-T mode. 1 = Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one. **0** = Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one.
10	0	R/W	**Port Type.** Since the VT6122 is a single port physical layer transceiver, bit 9.10 is set to "0" by default. When set to "1", this bit indicates a preference for operation as a MASTER. If the Link Partner does not indicate the same preference, the local PHY will operate as a MASTER, and the Link Partner will be a SLAVE. Otherwise, the normal MASTER/SLAVE assignment protocol is used. 1 = Multi-port device **0** = Single-port device
9	1	R/W	1**000BASE-T FDX Capability.** Since the VT6122 is 1000BASE-T FDX capable, this bit is "1" by default. If bit 9.9 is written to be "0", the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T FDX. Note that the Link Partner will be notified of the state of 9.9 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted. 1 = PHY is 1000BASE-T FDX capable
8	1	R/W	**1000BASE-T HDX Capability.** Since the VT6122 is 1000BASE-T HDX capable, this bit is "1" by default. If bit 9.8 is written to be "0", the Auto-Negotiation state machine for the local PHY will be blocked from advertising 1000BASE-T HDX. Note that the Link Partner will be notified of the state of 9.8 during Auto-Negotiation. After Auto-Negotiation is complete, changing the state of this bit has no effect unless Auto-Negotiation is manually restarted. 1 = PHY is 1000BASE-T HDX capable
7:0	0	R/W	**Reserved**

*Note***:** The state of this register is internally latched when the Auto-Negotiation state machine enters the ABILITY_DETECT state. Changes to the states of these bits are recognized only at that time. This register is valid only in 1000BASE-T mode.

Transmitter/Receiver Test Mode

Table 7. 1000BASE-T Transmitter/Receiver Test Modes

Bit 1 (9.15)	Bit 2 (9.14)	Bit 3 (9.13)	Test Mode
0	0	0	Normal operation
0	0	1	Test Mode 1 – Transmit waveform test
0	1	0	Test Mode 2 – Transmit jitter test in MASTER mode
0	1	1	Test Mode 3 – Transmit jitter test in SLAVE mode
1	0	0	Test Mode 4 – Transmitter distortion test
1	0	1	Reserved; operation not defined
1	1	0	Reserved; operation not defined
1	1	1	Reserved; operation not defined

- **Test Mode 1:** The PHY repeatedly transmits the following sequence of data symbols from all four transmitters: {{"+2" followed by 127 "0" symbols}, {"-2" followed by 127 "0" symbols}, {"+1" followed by 127 "0" symbols}, {"-1" followed by 127 "0" symbols}, {128 "+2" symbols, 128 "-2" symbols, 128 "+2" symbols, 128 "-2" symbols}, {1024 "0" symbols}}. The transmitter should use a 125.00 MHz 0.01% clock and should operate in MASTER timing mode.
- **Test Mode 2:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz 0.01% clock in the MASTER timing mode.
- **Test Mode 3:** The PHY transmits the data symbol sequence {+2, -2} repeatedly on all channels. The transmitter should use a 125.00 MHz 0.01% clock and should operate in SLAVE timing mode.
- **Test Mode 4:** The PHY transmits the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

  The maximum-length shift register used to generate the sequences defined by this polynomial is updated once per symbol interval (8ns). The bits stored in the shift register delay line at a particular time *n* are denoted by Scrn[10:0]. At each symbol period, the shift register is advanced by one bit, and one new bit represented by Scrn[0] is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive-OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, $x1_n$, and $x2_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the quinary symbols, s_n, as shown in Table 8. The transmitter should use a 125.00 MHz 0.01% clock and should operate in MASTER timing mode.

Table 8. 1000BASE-T Transmitter/Receiver Test Mode 4 – Quinary Symbols

$x2_n$	$x1_n$	$x0_n$	Quinary Symbol, s_n
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	-1
1	0	0	0
1	0	1	1
1	1	0	-2
1	1	1	-1

Offset 0Ah: 1000BASE-T Status Register

Bit	Default	Type	Description
15	0	RO LH SC	**MASTER/SLAVE Configuration Fault**. This bit indicates whether a MASTER/SLAVE configuration fault has been detected by the local PHY. A configuration fault occurs if both the local and remote PHYs are forced to the same MASTER/SLAVE state, or if no resolution is reached after seven retries. When such a fault has been detected, this bit is set to "1", but the PHY continues to renegotiate until the MASTER/SLAVE configuration is resolved. Once set, this bit is automatically cleared when (and only when) Register 10 is read. 1 = MASTER/SLAVE configuration fault detected **0** = No MASTER/SLAVE configuration fault detected
14	1	RO	**MASTER/SLAVE Configuration Resolution.** By default, the MASTER/SLAVE configuration is determined as part of the Auto-Negotiation process. However, the MASTER/SLAVE status can optionally be manually forced via bits in MII Register 9. Bit 10.14 indicates the final MASTER/SLAVE configuration status for the local PHY. This bit can change state only as a result of the reset or subsequent restart of the Auto-Negotiation process. This bit is only valid when the Auto-Negotiation Complete bit (1.5) is set. **1** = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	0	RO	**Local Receiver Status**. This bit indicates the state of the loc_rcvr_status flag within the PMA receive function within the local PHY. 1 = Local receiver OK (loc_rcvr_status == OK) **0** = Local receiver not OK (loc_rcvr_status == NOT_OK)
12	0	RO	**Remote Receiver Status**. This bit indicates the state of the rem_rcvr_status flag within the PMA receive function within the local PHY. 1 = Remote receiver OK (rem_rcvr_status == OK) **0** = Remote receiver not OK (rem_rcvr_status == NOT_OK)
11	0	RO	**LP 1000BASE-T FDX Capability.** This bit is set to "1" if the Link Partner PHY advertises 1000BASE-T FDX capability; otherwise, this bit is set to "0". 1 = LP 1000BASE-T FDX capable **0** = LP not 1000BASE-T FDX capable
10	0	RO	**LP 1000BASE-T HDX Capability**. This bit is set to "1" if the Link Partner PHY advertises 1000BASE-T HDX capability; otherwise, this bit is set to "0". 1 = LP is 1000BASE-T HDX capable **0** = LP is not 1000BASE-T HDX capable
9:8	0	RO	**Reserved**
7:0	0	RO SC	**Idle Error Count**. These bits indicate the Idle Error count, where 10.7 is the most significant bit. These bits contain a cumulative count of the errors detected when the receiver is receiving idles and PMA_TXMODE.indicate is equal to SEND (indicating that both the local and remote receiver status have been detected to be OK). The counter is incremented every symbol period that rx_error_status in the PMA receive function is equal to ERROR. Bits 10.7:0 are reset to all "0"s when the error count is read by the management function, or upon execution of the PCS reset function, and they are saturated to all "1"s in case of overflow. This bit applies only in 1000BASE-T mode.

Note: **The bits in this register apply only when the Page Received bit (6.1) is set..**

Offset 0Bh: Reserved Register

Bit	Default	Type	Description
15:0	0	RO	**Reserved**

Offset 0Ch: Reserved Register

Bit	Default	Type	Description
15:0	0	RO	**Reserved**

Offset 0Dh: Reserved Register

Bit	Default	Type	Description
15:0	0	RO	**Reserved**

Offset 0Eh: Reserved Register

Bit	Default	Type	Description
15:0	0	RO	**Reserved**

Offset 0Fh: 1000BASE-T Status Extension Register #1

Bit	Default	Type	Description
15	0	RO	**1000BASE-X FDX Capability.** The VT6122 is not 1000BASE-X capable, so this bit is hard-wired to "0". 1 = PHY is 1000BASE-X FDX capable **0** = PHY is not 1000BASE-X FDX capable
14	0	RO	**1000BASE-X HDX Capability.** The VT6122 is not 1000BASE-X capable, so this bit is hard-wired to "0". 1 = PHY is 1000BASE-X HDX capable **0** = PHY is not 1000BASE-X HDX capable
13	1	RO	**1000BASE-T FDX Capability.** The VT6122 is 1000BASE-T FDX capable, so this bit is hard-wired to "1". **1** = PHY is 1000BASE-T FDX capable 0 = PHY is not 1000BASE-T FDX capable
12	1	RO	**1000BASE-T HDX Capability.** The VT6122 is 1000BASE-T HDX capable, so this bit is hard-wired to "1". **1** = PHY is 1000BASE-T HDX capable 0 = PHY is not 1000BASE-T HDX capable
11:0	0	RO	**Reserved**

Offset 10h: 100BASE-TX Status Extension Register

Bit	Default	Type	Description
15	0	RO	**100BASE-TX Descrambler Locked.** This bit is set to "1" when the 100BASE-TX descrambler is locked; otherwise, this bit is set to "0". 1 = Descrambler locked **0** = Descrambler not locked
14	0	RO SC	**100BASE-TX Lock Error Detected.** This bit is set to "1" if the 100BASE-TX descrambler has lost lock since the last read of this bit; otherwise, this bit is set to "0". 1 = Lock error detected since last read **0** = Lock error not detected since last read
13	0	RO SC	**100BASE-TX Disconnect State.** This bit is set to "1" if the 100BASE-TX connection has been broken since the last read of this bit; otherwise, this bit is set to "0". 1 = PHY 100BASE-TX link disconnected **0** = PHY 100BASE-TX link not disconnected
12	0	RO	**100BASE-TX Current Link Status**. This bit is set to "1" if the 100BASE-TX link is active; otherwise, this bit is set to "0". 1 = PHY 100BASE-TX link active **0** = PHY 100BASE-TX link inactive
11	0	RO SC	**100BASE-TX Receive Error Detected**. This bit is set to "1" if a 100BASE-TX packet with an invalid code has been received since the last read of this bit; otherwise, this bit is set to "0". 1 = Receive error detected since last read **0** = Receive error not detected since last read
10	0	RO SC	**100BASE-TX Transmit Error Detected.** This bit is set to "1" if a 100BASE-TX packet has been received with a transmit error code since the last read of this bit; otherwise, this bit is set to "0". 1 = Transmit error detected since last read 0 = Transmit error not detected since last read
9	0	RO SC	**100BASE-TX False Carrier (SSD Error) Detected**. This bit is set to "1" if a 100BASE-TX false carrier (Start-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0". 1 = SSD error detected since last read **0** = SSD error not detected since last read
8	0	RO SC	**100BASE-TX Premature End (ESD Error) Detected.** This bit is set to "1" if a 100BASE-TX premature end (End-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0". Apply only in 100BASE-TX mode. 1 = ESD error detected since last read **0** = ESD error not detected since last read
7:0	0	RO	**Reserved**

Note: **The bits in this register apply only in 100BASE-TX mode.**

Offset 11h: 1000BASE-T Status Extension Register #2

Bit	Default	Type	Description
15	0	RO	**1000BASE-T Descrambler Locked**. This bit is set to "1" when the 1000BASE-T descrambler is locked; otherwise, this bit is set to "0". 1 = Descrambler locked **0** = Descrambler not locked
14	0	RO SC	**1000BASE-T Lock Error Detected.** This bit is set to "1" if the 1000BASE-T descrambler has lost lock since the last read of this bit; otherwise, this bit is set to "0". 1 = Lock error detected since last read **0** = Lock error not detected since last read
13	0	RO SC	**1000BASE-T Disconnect State.** This bit is set to "1" if the 1000BASE-T connection has been broken since the last read of this bit; otherwise, this bit is set to "0". 1 = PHY 1000BASE-T link disconnected **0** = PHY 1000BASE-T link not disconnected
12	0	RO	**1000BASE-T Current Link Status.** This bit is set to "1" if the 1000BASE-T link is active; otherwise, this bit is set to "0". 1 = PHY 1000BASE-T link active **0** = PHY 1000BASE-T link inactive
11	0	RO SC	**1000BASE-T Receive Error Detected**. This bit is set to "1" if a 1000BASE-T packet with an invalid code has been received since the last read of this bit; otherwise, this bit is set to "0". 1 = Receive error detected since last read **0** = Receive error not detected since last read
10	0	RO SC	**1000BASE-T Transmit Error Detected**. This bit is set to "1" if a 1000BASE-T packet has been received with a transmit error code since the last read of this bit; otherwise, this bit is set to "0". 1 = Transmit error detected since last read **0** = Transmit error not detected since last read
9	0	RO SC	**1000BASE-T False Carrier (SSD Error) Detected.** This bit is set to "1" if a 1000BASE-T false carrier (Start-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0". 1 = SSD error detected since last read **0** = SSD error not detected since last read
8	0	RO SC	**1000BASE-T Premature End (ESD Error) Detected**. This bit is set to "1" if a 1000BASE-T premature end (End-of-Stream Delimiter error) has been detected since the last read of this bit; otherwise, this bit is set to "0". 1 = ESD error detected since last read **0** = ESD error not detected since last read
7	0	RO SC	**1000BASE-T Carrier Extension Error Detected**. This bit is set to "1" if a carrier extension error has been detected since the last read of this bit; otherwise, this bit is set to "0". 1 = Carrier extension error detected since last read **0** = Carrier extension error not detected since last read
6	0	RO	**Non-compliant BCM5400 Detected.** This bit is a read-only bit set to "1" if the VT6122 detects a non-compliant BCM5400 as its link partner; otherwise, this bit is set to "0". This bit is valid only when the 1000BASE-T descrambler has achieved a locked state. The behavior of the PHY with regard to non-compliant BCM5400 detection is controlled by MII Register bits 18.7 and 18.6. 1 = Non-compliant BCM5400 detected **0** = Non-compliant BCM5400 not detected
5:0	0	RO	**Reserved**

***Note*:** The bits in this register apply only in 1000BASE-T mode.

Offset 12h: Bypass Control Register

Bit	Default	Type	Description
15	0	R/W	**Transmit Disable**. When this bit is set to "1", the transmitter outputs are left floating (high impedance). 1 = Transmitter disabled in PHY **0** = Transmitter enabled
14	0	R/W	**Bypass 4B5B Encoder/Decoder**. When this bit is set to "1", the 5B codes (TX_ER and TXD[4:0]) will be passed from the MII interface directly to the scrambler, bypassing the 4B5B encoder. Note that in this mode, J/K and T/R code insertion will not be performed. The receiver will pass descrambled/aligned 5B codes directly to the MII interface (RX_ER and RXD[4:0]), bypassing the 4B5B decoder. Carrier sense (CRS) is still asserted when a valid frame is detected. This bit applies only in 100BASE-TX mode. 1 = Bypass 4B5B encoder/decoder **0** = Enable 4B5B encoder/decoder
13	0	R/W	**Bypass Scrambler**. When this bit is set to "1", the scrambler is disabled. This bit applies only in 100BASE-TX and 1000BASE-T modes. 1 = Bypass scrambler **0** = Enable scrambler
12	0	R/W	**Bypass Descrambler**. When this bit is set to "1", the descrambler is disabled. This bit applies only in 100BASE-TX and 1000BASE-T modes. 1 = Bypass descrambler **0** = Enable descrambler
11	0	R/W	**Bypass PCS Receive.** When this bit is set to "1", PCS receive for the four subchannels is bypassed. In 1000BASE-T mode, a 4-D symbol is encoded into a 10-bit data word and sent to the GMII interface. The RX_DV and RX_ER pins are used for the upper two bits of the encoded data, and RXD pins are used for the remaining eight bits of the encoded data. When receiving idle codes, the Viterbi decoder can by bypassed, receiving symbols through the 4-D slicer instead. In 100BASE-TX mode, to pass the unaligned symbols directly to the MII interface, this control bit should be set only when the 4B5B decoder is also bypassed. 1 = Bypass PCS receive **0** = Enable PCS receive
10	0	R/W	**Bypass PCS Transmit**. When this bit is set to "1", the PCS transmit for the four subchannels is bypassed. 1 = Bypass PCS transmit **0** = Enable PCS transmit
9	0	R/W	**Bypass LFI Timer**. If this bit is set, the link_fail_inhibit timer defined in Clause 28 of the IEEE 802.3 standard is bypassed under certain conditions to allow faster re-Auto-Negotiation. This timer will be bypassed if either the MASTER/SLAVE negotiation resulted in a tie, or no common capabilities were discovered during the previous negotiation. If this bit is not set, the Auto-Negotiation state machines behave as defined in the IEEE standard. 1 = Bypass link_fail_inhibit timer (to enable faster Auto-Negotiation) **0** = Do not bypass link_fail_inhibit timer
8	0	R/W	**Enable Transmit Clock TX_TCLK Output on LED4 Pin**. When this bit is written to a "1", the LED4 output pin becomes a test pin for the transmit clock "TX_TCLK" of the PHY port. This capability is intended to enable measurement of transmitter timing jitter, as specified in IEEE Standard 802.3-2002, section 40.6.1.2.5. When in IEEE-specified transmitter test modes 2 or 3 (see IEEE 802.3-2002, section 40.6.1.1.2 and MII Register bits 9.15:13), the peak-to-peak jitter of the zero-crossings of the differential signal output at the MDI, relative to the corresponding edge of TX_TCLK, is measured. The corresponding edge of TX_TCLK is the edge of the transmit test clock, in polarity and time, that generates the zero-crossing transition being measured. 1 = Enable TX_TCLK test output on LED4 pin **0** = Disable TX_TCLK test output on LED4 pin
7	0	R/W	**Force Non-compliant BCM5400 Detection.** When this bit is set to a "1" and MII Register bit 18.6 is set to a "1", then the VT6122 operates as a non-compliant BCM5400 PHY. If MII Register bit 18.6 is set to a "1" and this bit is a "0", then the VT6122 operates as a fully IEEE compliant PHY. If MII Register bit 18.6 is set to "0", then this bit has no affect on the VT6122 operation. This bit applies only in 1000BASE-T mode. 1 = Force non-compliant BCM5400 detection **0** = Do not force non-compliant BCM5400 detection

Bit	Default	Type	Description
6	0	R/W RS	**Bypass Non-compliant BCM5400 Detection.** When this bit is set to "0", the PHY automatically detects and corrects for non-compliant BCM5400 link partner PHYs. When this bit is set to "1", automatic non-compliant BCM5400 detection is disabled, and the local PHY's operating mode is determined by the status of MII Register bit 18.7. If bit 18.7 is a "1", then the local PHY operates as a non-compliant BCM5400 PHY. When bit 18.7 is a "0", the local PHY operates as a fully IEEE-compliant PHY. Note that this control bit applies only in 1000BASE-T mode. 1 = Disable automatic non-compliant BCM5400 detection **0** = Enable automatic non-compliant BCM5400 detection
5	0	R/W	**Disable Automatic Pair Swap Correction.** When this bit is set to "0", the PHY automatically corrects pair swaps between subchannels A and B, and between subchannels C and D, due to "MDI/MDI-X crossover". It will also correct pair swaps between subchannels C and D due to cabling errors. When this bit is set to "1", the PHY does not correct pair swaps. Note that this control bit applies in all modes: 10BASE-T, 100BASE-TX, and 1000BASE-T.[2] 1 = Disable pair swap correction **0** = Enable pair swap correction
4	0	R/W	**Disable Polarity Correction**. This bit is valid only in 1000BT mode. When this bit is set to "0", the PHY automatically corrects polarity inversion on all the sub-channels. When this bit is set to "1", the PHY does not compensate for polarity inversion. In 100BT mode, polarity inversion correction is not necessary (100BT is insensitive to cable polarity).In 10BT mode, polarity inversion correction is always done regardless of the state this bit.
3	1	R/W RS	**Parallel-Detect Control.** When this bit is "1", MII Register 4, bits [8:5], are taken into account when attempting to parallel-detect. This is the default behavior expected by the standard. Setting this bit to a "0" will result in Auto-Negotiation ignoring the advertised abilities, as specified in MII Register 4, during parallel detection of a non-auto-negotiating 10BASE-T or 100BASE-TX PHY. **1** = Do not ignore advertised ability 0 = Ignore advertised ability
2	0	R/W	**Disable Pulse Shaping Filter.** When this bit is set to "1", the 1000BASE-T two-tap digital transmit filter is disabled. This bit applies only in 1000BASE-T mode. 1 = Disable pre-emphasis filter **0** = Enable pre-emphasis filter
1	0	R/W RS	**Disable Automatic 1000BASE-T Next-Page Exchanges.** This bit is used to control the automatic exchange of 1000BASE-T Next-Pages defined in IEEE 802.3 - 2002 (Annex 40C). When this bit is set, the automatic exchange of these pages is disabled, and the control is returned to the user through the SMI after the base page has been exchanged. The user then has complete responsibility to: • send the correct sequence of Next-Pages to the Link Partner, and • determine common capabilities and force the device into the correct configuration following successful exchange of pages. When bit 18.1 is reset to "0", the 1000BASE-T related Next-Pages are automatically exchanged without user intervention. If the Next Page bit 4.15 was set by the user in the Auto-Negotiation Advertisement register at the time the Auto-Negotiation was restarted, control is returned to the user for additional Next-Pages following the 1000BASE-T Next-Page exchange. If both 18.1 and 4.15 are reset when an Auto-Negotiation sequence is initiated, all Next-Page exchange is automatic, including sourcing of null pages. No user notification is provided until either Auto-Negotiation completes or fails. See the description of Register bit 4.15 for more details on standard Next-Page exchanges. Note that this control bit applies only in 1000BASE-T mode. 1 = Disable automatic 1000BASE-T Next-Page exchanges **0** = Enable automatic 1000BASE-T Next-Page exchanges
0	0	-	**Reserved**

[2]Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

Offset 13h: Receive Error Counter Register

Bit	Default	Type	Description
15:8	0	RO	**Reserved**
7:0	0	RO SC	**Receive Error Counter**. This register represents the number of non-collision packets with receive errors since last read. Each time the PHY detects a non-collision packet containing at least one error, the counter is incremented. The counter will saturate at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.

Offset 14h: False Carrier Sense Counter Register

Bit	Default	Type	Description
15:8	0	RO	**Reserved**
7:0	0	RO SC	**False Carrier Sense Counter**. The PHY will increment this register each time it detects a false carrier on the receive input. The counter will saturate at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes. Number of false carrier events since last read

Offset 15h: Disconnect Counter Register

Bit	Default	Type	Description
15:8	0	RO	**Reserved**
7:0	0	RO SC	**Disconnect Counter.** The PHY will increment this register each time the Carrier Integrity Monitor (CIM) enters the “link unstable” state. The counter will saturate at 0FFh. This register is cleared only when read, or upon a hardware or software reset. Number of disconnects since last read

Offset 16h: 10BASE-T Control & Status Register[3]

Bit	Default	Type	Description
15	0	R/W RS	**Disable Link Integrity Test State Machine.** When this bit is set to "0", the VT6122 link integrity state machine runs automatically; it also controls link pass status. When this bit is set to "1", the link integrity state machine is bypassed, and the PHY is forced into link pass status. 1 = Disable link integrity test **0** = Enable link integrity test
14	0	R/W RS	**Disable Jabber Detect.** When this bit is set to "0", the VT6122 automatically shuts off the transmitter when a transmission request exceeds the IEEE-specified time limit. When this bit is set to "1", transmission requests are allowed to be arbitrarily long without shutting down the transmitter. 1 = Disable jabber detect **0** = Enable jabber detect
13	0	R/W RS	**Disable Echo Mode.** When this bit is set to "1", the logical state of the TX_EN pin will not echo onto the CRS signal, effectively disabling CRS from being asserted in half-duplex operation. For example, when TX_EN is driven to "0", the CRS signal will also be driven to a "0". When this bit is set to "0", the TX_EN pin will be echoed onto the CRS signal. 1 = Disable echo mode **0** = Enable echo mode
12	0	R/W RS	**SQE Disable**. When this bit is set to "1", SQE (Signal Quality Error) pulses are not sent. Note that this control bit applies in 10BASE-T HDX mode only. 1 = Disable SQE transmit **0** = Enable SQE transmit
11:10	00	R/W RS	**Squelch Control.** When these bits are set to "00", the VT6122 uses 300mV as the squelch threshold level, prescribed by the IEEE's 10BASE-T specification. When these bits are set to "01", the squelch level is decreased to 197mV, which may improve the bit error rate performance on long loops. When these bits are set to "10", the squelch level is increased to 450mV, which may improve the bit error rate in high-noise environments. These bits also control the ActiPHY™ comparator squelch levels (see Section 15.9: "ActiPHY™ Power Management" for more information). **00** = 300mV 01 = 197mV 10 = 450mV 11 = Reserved
9	0	R/W	**Reserved**
8	0	RO SC	**EOF Error**. When this bit returns a "1", a defective EOF (End-of-Frame) sequence has been received since the last time this bit was read. This bit is automatically set to "0" when it is read[4]. 1 = EOF error detected since last read **0** = EOF error not detected since last read
7	0	RO SC	**10BASE-T Disconnect State**. This bit is set to "1" if the 10BASE-T connection has been broken by the Carrier Integrity Monitor (CIM) since the last read of this bit; otherwise, this bit is set to "0". 1 = 10BASE-T link disconnected **0** = 10BASE-T link connected
6	0	RO	**10BASE-T Link Status**. This bit is set to "1" if the 10BASE-T link is active; otherwise, this bit is set to "0". 1 = 10BASE-T link active **0** = 10BASE-T link inactive
5:3	000	R/W RS	**Current Reference Trim.** These bits provide trim adjustments for the internal current reference on the VT6122. This adjustment controls the transmit power only in 10BASE-T mode. It may be used, in particular, to trim the nominal transmit power for a particular network interface design. It has no effect on the receive operation of the VT6122. The current reference trim adjustments are encoded using the bit values in Table 9.
2:1	00	RO	**CRS behavior control**. These bits used to select CRS behavior according to the following table used to select CRS behavior according to Table 10.
0	-	-	**Reserved**

[3]The bits in this register apply only in 10BASE-T mode, except for bit 22.13, which applies to both 10BASE-T and 100BASE-TX modes.
[4]The bits in this register apply only in 10BASE-T mode, except for bit 22.13, which applies to both 10BASE-T and 100BASE-TX modes.

Table 9. 10BASE-T Current Reference Trim Values

Bits 5:3	Adjustment
011	+6%
010	+6%
001	+4%
000	+2%
111	0%
110	-2%
101	-4%
100	-4%

Table 10. CRS Behavior Selected by Offset 16h Bit[2:1]

	CRS control			
	2'b00 (default)	2'b01	2'b10	2'b11
1000 FULL	CRS=RXDV	CRS=0	CRS=RXDV	CRS=0
1000 HALF	CRS=RXDV+TXEN	CRS=RXDV+TXEN	CRS=RXDV	CRS=RXDV
100 FULL	CRS=RXDV	CRS=0	CRS=RXDV	CRS=0
100 HALF	CRS=RXDV+TXEN	CRS=RXDV+TXEN	CRS=RXDV	CRS=RXDV
10 FULL	CRS=RXDV	CRS=0	CRS=RXDV	CRS=0
10 HALF	CRS=RXDV+TXEN	CRS=RXDV+TXEN	CRS=RXDV	CRS=RXDV

Offset 17h: Extended PHY Control Register #1

Bit	Default	Type	Description
15:6	0h	R/W RS	**Reserved**
5	0	R/W	**ActiPHY™ Enable**. The Station Manager is expected to set this bit to "1" when it detects that the PHY has not established a link for a certain period of time, thus enabling the ActiPHY™ power management mode. This bit is cleared when the PHY detects network activity. See Functional Description "ActiPHY™ Power Management" for more information. 1 = ActiPHY™ low power mode enabled **0** = ActiPHY™ low power mode disabled
4:3	00	R/W	**Reserved**
2, 0	00	RO	**Reserved**
1	0	R/W	**Reserved**

Offset 18h: Extended PHY Control Register #2

Bit	Default	Type	Description
15:13	111	R/W RS	**100/1000BASE-T Edge Rate Control.** These bits control the transmit driver slew rate in 100BASE-TX and 1000BASE-T modes only, as shown above. The difference between each setting is approximately 200ps to 300ps, with the "+3" setting resulting in the slowest edge rate, and the "-4" setting resulting in the fastest edge rate. 011 = +3 edge rate (slowest) 010 = +2 edge rate 001 = +1 edge rate **000** = Nominal edge rate 111 = -1 edge rate 110 = -2 edge rate 101 = -3 edge rate 100 = -4 edge rate (fastest)
12:10	000	R/W RS	**100/1000BASE-T Transmit Voltage Reference Trim**. These bits provide trim adjustments for the internal voltage reference on the VT6122. This adjustment controls the transmit power for 100BASE-TX and 1000BASE-T modes. It may be used, in particular, to trim the nominal transmit power for a particular network interface design. (See Table 11)
9:7	100	R/W RS	**Reserved**
6:4	100	R/W	**Reserved**
3:1	000	RO	**Cable Quality Status**. Valid only in 100/1000BASE-T modes, these bits indicate the approximate effective electrical length of the cable in meters, as shown in the register table above. **000** = cable length < 10m 001 = 10m < cable length < 20m 010 = 20m < cable length < 40m 011 = 40m < cable length < 80m 100 = 80m < cable length < 100m 101 = 100m < cable length <140m 110 = 140m < cable length <180m 111 = cable length > 180m
0	0	R/W	**1000BASE-T Analog Loopback Control.** This bit is valid only in 1000BASE-T mode. When asserted, this bit enables analog loopback through the VT6122's internal hybrid. Because loopback occurs at the hybrid, the transmit/receive signal will be observed on the media (cable). This bit should always be disabled in normal operating modes. Additionally, the integrate PHY must be programmed through a certain sequence of MII register writes for analog loopback to function. See MII Register bit 0.14 for information about the IEEE - 802.3 standard's specified loopback operation. 1 = Enable 1000BASE-T analog loopback through the hybrid **0** = Disable 1000BASE-T analog loopback through the hybrid

The transmit voltage reference trim adjustments are encoded using the bit values in the following table:

Table 11. 100/1000BASE-T Transmit Voltage Reference Trim Values

Bits 12:10	Adjustment
011	+6%
010	+6%
001	+4%
000	+2%
111	0%
110	-2%
101	-4%
100	-4%

Offset 19h: Interrupt Mask Register

Bit	Default	Type	Description
15	0	R/W	**Interrupt Pin Enable.** When this bit is set to "1", the hardware interrupt is enabled, meaning that the state of the external interrupt pin (MDINT#, which is active low) can be influenced by the state of the Interrupt Status bit (26.15). When this bit is set to "0", the interrupt status bits (Register 26:14-0) continue to be set in response to interrupts, but the interrupt hardware pin MDINT# on the VT6122 will not be influenced by the PHY. The INTA# hardware pin is essentially a logical NAND function of the register bits (25.15 and 26.15). An INTA# can be asserted only if Register bit 25.15 is set to "1", and an interrupt is pending (pending interrupts are indicated by Register 26.15). 1 = Enable interrupt pin **0** = Disable interrupt pin
14	0	R/W RS	**Speed State-Change Interrupt Mask.** 1 = Enable Speed interrupt **0** = Disable Speed interrupt
13	0	R/W RS	**Link State-Change / ActiPHY™ Interrupt Mask**. While bit 23.5 is set, setting this bit to "1" enables the ActiPHY™ interrupt. While bit 23.5 is cleared, setting this bit to "1" enables the Link State-Change interrupt. 1 = Enable Link / ActiPHY™ interrupt **0** = Disable Link / ActiPHY™ interrupt
12	0	R/W RS	**Duplex State-Change Interrupt Mask** 1 = Enable Duplex interrupt **0** = Disable Duplex interrupt
11	0	R/W RS	**Auto-Negotiation Error Interrupt Mask** 1 = Enable Auto-Negotiation Error interrupt **0** = Disable Auto-Negotiation Error interrupt
10	0	R/W RS	**Auto-Negotiation-Done Interrupt Mask** 1 = Enable Auto-Negotiation-Done interrupt **0** = Disable Auto-Negotiation-Done interrupt
9	0	R/W RS	**Page-Received Interrupt Mask**. [5] 1 = Enable Page-Received interrupt **0** = Disable Page-Received interrupt
8	0	R/W RS	**Symbol Error Interrupt Mask**. 1 = Enable Symbol Error interrupt **0** = Disable Symbol Error interrupt
7	0	R/W RS	**Descrambler Lock-Lost Interrupt Mask.** 1 = Enable Lock-Lost interrupt **0** = Disable Lock-Lost interrupt
6	0	R/W RS	**MDI-Crossover Change Interrupt Mask.**[6] When this bit is set to "1", the MDI Crossover Change interrupt is enabled. 1 = Enable MDI Crossover change interrupt **0** = Disable MDI Crossover change interrupt
5	0	R/W RS	**Polarity-Change Interrupt Mask.** 1 = Enable Polarity-Change interrupt **0** = Disable Polarity-Change interrupt
4	0	R/W RS	**Jabber-Detect Interrupt Mask.** This bit applies only in 10BASE-T mode. 1 = Enable Jabber-Detect interrupt **0** = Disable Jabber-Detect interrupt
3	0	R/W RS	**False Carrier Interrupt Mask**. 1 = Enable False Carrier interrupt **0** = Disable False Carrier interrupt
2	0	R/W RS	**Parallel-Detect Error Interrupt Mask**. 1 = Enable Parallel-Detect interrupt **0** = Disable Parallel-Detect interrupt

[5] This bit applies only in 100BASE-TX and 1000BASE-T modes.

[6] Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

Bit	Default	Type	Description
1	0	R/W RS	**MASTER/SLAVE Resolution Error Interrupt Mask**. This bit applies only in 1000BASE-T mode. 1 = Enable MASTER/SLAVE interrupt **0** = Disable MASTER/SLAVE interrupt
0	0	R/W RS	**RX_ER Interrupt Mask** 1 = Enable RX_ER interrupt **0** = Disable RX_ER interrupt

Offset 1Ah: Interrupt Status Register

Bit	Default	Type	Description
15	0	RO SC	**Interrupt Status**. When this bit is set to "1", an unacknowledged interrupt is pending. The cause of the interrupt can be determined by reading the interrupt status bits in this register. This bit is automatically cleared when read. (NOTE: interrupts can be pending only if bit 25.15 is set) 1 = Interrupt pending **0** = No interrupt pending
14	0	RO SC	**Speed State-Change Interrupt Status**. When the operating speed of the PHY changes, this bit is set to "1" only if bit 25.14 is also set to "1". This bit is automatically cleared when read. 1 = Speed interrupt pending
13	0	RO SC	**Link State-Change / ActiPHY™ Interrupt Status.** While bit 23.5 is set, this bit is set to "1" when energy is detected on the media interface. When bit 23.5 is cleared, this bit is set to "1" when the link status of the PHY changes. This bit is set to "1" only if bit 25.13 is also set to "1". This bit is automatically cleared when read. 1 = Link state-change / ActiPHY™ interrupt pending
12	0	RO SC	**Duplex State-Change Interrupt Status.** When the duplex status of the PHY changes, this bit is set to "1" if bit 25.12 is also set to "1". This bit is automatically cleared when read. 1 = Duplex interrupt pending
11	0	RO SC	**Auto-Negotiation Error Interrupt Status**. When an error is detected by the Auto-Negotiation state machine, this bit is set to "1" if bit 25.11 is also set to "1". This bit is automatically cleared when read. 1 = Auto-Negotiation Error interrupt pending
10	0	RO SC	**Auto-Negotiation-Done Interrupt Status**. When the Auto-Negotiation state machine finishes a negotiation process, this bit is set to "1" if bit 25.10 is also set to "1". This bit is automatically cleared when read. 1 = Auto-Negotiation-Done interrupt pending
9	0	RO SC	**Page-Received Interrupt Status**. When a new Next-Page is received, this bit is set to "1" if bit 25.9 is also set to "1". This bit is automatically cleared when read. 1 = Page-Received Interrupt pending
8	0	RO SC	**Symbol Error Interrupt Status.** When a symbol error is detected by the descrambler, this bit is set to "1" if bit 25.8 is also set to "1". This bit is automatically cleared when read. This bit applies only in 100BASE-TX and 1000BASE-T modes. 1 = Symbol Error interrupt pending
7	0	RO SC	**Descrambler Lock-Lost Interrupt Status**. When the descrambler loses lock, this bit is set to "1" if bit 25.7 is also set to "1". This bit is automatically cleared when read. 1 = Lock-Lost interrupt pending
6	0	RO SC	**MDI Crossover Change Interrupt Status**[7]**.** When the MDI crossover change status of the PHY changes, this bit is set to "1" if bit 25.6 is also set to "1". This bit is automatically cleared when read. 1 = MDI Crossover interrupt pending
5	0	RO SC	**Polarity-Change Interrupt Status**. When a polarity status error of the PHY changes, bit this is set to "1" if bit 25.5 is also set to "1". This bit is automatically cleared when read. 1 = Polarity-Change interrupt pending
4	0	RO SC	**Jabber-Detect Interrupt Status**. When "jabber" is detected, this bit is set to "1" if bit 25.4 is also set to "1". This bit is automatically cleared when read. This bit applies only in 10BASE-T mode. 1 = Jabber-Detect interrupt pending
3	0	RO SC	**False Carrier Interrupt Status**. When a false carrier is detected, this bit is set to "1" if bit 25.3 is also set to "1". This bit is automatically cleared when read. 1 = False Carrier interrupt pending
2	0	RO SC	**Parallel-Detect Error Interrupt Status**. When a Parallel-Detect error is detected, this bit is set to "1" if bit 25.2 is also set to "1". This bit is automatically cleared when read. 1 = Parallel-Detect Error interrupt pending
1	0	RO SC	**MASTER/SLAVE Resolution Error Interrupt Status**. When a MASTER/SLAVE resolution error is detected, this bit is set to "1" if bit 25.1 is also set to "1". This bit is automatically cleared when read. This bit applies only in 1000BASE-T mode. 1 = MASTER/SLAVE Error interrupt pending

[7] Consistent with 10/100/1000BASE-T PHYs on the market today, this bit applies only when Auto-Negotiation is enabled; Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

Bit	Default	Type	Description
0	0	RO	**RX_ER Interrupt Status.** When an RX_ER condition occurs, this bit is set to "1". This bit is automatically cleared when read. 1 = RX_ER interrupt pending 0 = No RX_ER interrupt pending

Offset 1Bh: Parallel LED Control Register

Bit	Default	Type	Description
15	0	R/W	**Link10 LED Force On**[8]**.** When this bit is set to "1", the Link10 LED status bit is asserted. This control bit has effect only if the corresponding LED status bit is enabled. 1 = Link10 LED forced on **0** = Link10 LED not forced on
14	0	R/W RS	**Link10 LED Disable**[8] 1 = Disable Link10 LED **0** = Enable Link10 LED
13	0	R/W	**Link100 LED Force On**[8]. When this bit is set to "1", the Link100 LED status bit is asserted. 1 = Link100 LED forced on **0** = Link100 LED not forced on
12	0	R/W RS	**Link100 LED Disable**[8]**.** 1 = Disable Link100 LED **0** = Enable Link100 LED
11	0	R/W	**Link1000 LED Force On**[8]**.** When this bit is set to "1", the Link1000 LED status bit is asserted. 1 = Link1000 LED forced on **0** = Link1000 LED not forced on
10	0	R/W RS	**Link1000 LED Disable**[8]**.** 1 = Disable Link1000 LED **0** = Enable Link1000 LED
9	0	R/W	**Duplex LED Force On**[8]**.** 1 = Duplex LED forced on **0** = Duplex LED not forced on
8	0	R/W RS	**Duplex LED Disable**[8]**.** 1 = Disable Duplex LED 0 = Enable Duplex LED
7	0	R/W	**Activity LED Force On**[8]**.** This control bit has effect only if the corresponding LED status bit is enabled. 1 = Activity LED forced on 0 = Activity LED not forced on
6	0	R/W RS	**Activity LED Disable**[8]**.** 1 = Disable Activity LED **0** = Enable Activity LED
5	0	R/W	**Reserved**
4	0	R/W RS	**Reserved**
3	0	R/W RS	**LED Pulse Enable.** When this bit is set to "1", the LED output signals are pulsed at 5KHz with a 20% duty cycle for low-power operation. 1 = Enable LED pulsing **0** = Disable LED pulsing (This bit is available in all four LED modes)
2	1	R/W RS	**Link/Acivity LED Blink Enable**[8]. This bit is only available while LED function is programmed in (PHYLED1, PHYLED0) = 2'b00 mode. When this bit is set to "1", the Link/Activity LED blink function is enabled. In the blinking state the Link/Activity LED operates as follows: - The LED is constantly on when the link is up and data is NOT being transmitted or received. - The LED will blink at the rate specified by bit 27.1 when the link is up AND data is either being transmitted or received. **1** = Enable Link/Acivity LED Blink 0 = Disable Link/Activity LED Blink

[8] These bits are available only while the LED function in MAC register 78 is programmed in (PHYLED1, PHYLED0) = 2'b00 mode

Bit	Default	Type	Description
1	0	R/W RS	**Link/Acivity LED Blink Rate**. This bit specifies the Link/Activity LED blink rate when bit 27.2 is set to "1". 0 = 10Hz blink rate 1 = 5 Hz blink rate (This bit is available in all four LED modes)
0	0	RO	**Reserved**

Offset 1Ch: Auxiliary Control & Status Register

Bit	Default	Type	Description
15	0	RO	**Auto-Negotiation Complete**. This bit is a copy of bit 1.5, duplicated here for convenience. 1 = Auto-Negotiation complete **0** = Auto-Negotiation not complete
14	0	RO	**Auto-Negotiation Disabled**. When this bit is read as a "1", this bit indicates that the Auto-Negotiation process has been bypassed. This happens only when Register bit 0.12 is set to "0". 1 = Auto-Negotiation was disabled **0** = Auto-Negotiation is enabled
13	0	RO	**MDI/MDI-X Crossover Indication.** When this bit returns a "1", the Auto-Negotiation state machine has determined that crossover does not exist in the signal path. The crossover will therefore be performed internally to the PHY, as described by the MDI/MDI-X crossover specification[9]. 1 = MDI/MDI-X crossover detected 0 = MDI/MDI-X crossover not detected
12	0	RO	**CD Pair Swap** [10]. When this bit returns a "1", the PHY has determined that subchannel cable pairs C and D have been swapped between the far-end transmitted and the receiver. When this bit returns a "1", the PHY internally swaps pairs C and D (as long as bit 18.5 is set to "0"). 1 = CD pairs are swapped **0** = CD pairs are not swapped
11	0	RO	**A Polarity Inversion**. This bit only applies in 1000BT mode. When this bit returns a "1", the PHY has determined that the polarity of sub-channel cable pair A has been inverted between the far-end transmitter and the near-end receiver. When this bit returns a "1", the PHY internally corrects the pair inversion (as long as bit 18.4 is set to "0"). In 10/100BT modes, this bit is always "0", regardless of whether polarity inversion correction takes place. 1 = Polarity swapped on pair A **0** = Polarity not swapped on pair B
10	0	RO	**B Polarity Inversion.** This bit only applies in 1000BT mode. When this bit returns a "1", the PHY has determined that the polarity of sub-channel cable pair B has been inverted between the far-end transmitter and the near-end receiver. When this bit returns a "1", the PHY internally corrects the pair inversion (as long as bit 18.4 is set to "0"). In 10/100BT modes, this bit is always "0", regardless of whether polarity inversion correction takes place. 1 = Polarity swapped on pair B **0** = Polarity not swapped on pair B
9	0	RO	**C Polarity Inversion**[11]. When this bit returns a "1", the PHY has determined that the polarity of subchannel cable pair C has been inverted between the far-end transmitter and the near-end receiver. When this bit returns a "1", the PHY internally corrects the pair inversion (as long as bit 18.4 is set to "0"). The state of this bit is valid only when bit 1.5 is set to "1". 1 = Polarity swapped on pair C **0** = Polarity not swapped on pair C
8	0	RO	**D Polarity Inversion**[11]. When this bit returns a "1", the PHY has determined that the polarity of subchannel cable pair D has been inverted between the far-end transmitter and the near-end receiver. When this bit returns a "1", the PHY internally corrects the pair inversion (as long as bit 18.4 is set to "0"). The state of this bit is valid only when bit 1.5 is set to "1". 1 = Polarity swapped on pair D **0** = Polarity not swapped on pair D
7:6	00	RO	**Reserved**
5	0	RO	**Duplex Status**. This bit indicates the actual FDX/HDX operating mode of the PHY. 1 = FDX **0** = HDX

[9]This bit is valid only after descrambler lock has been achieved.
[10]This bit is valid only in 1000BASE-T mode.
[11]This bit applies ony in 1000BASE-T mode.

Bit	Default	Type	Description
4:3	00	RO	**Speed Status.** These bits indicate the actual operating speed of the PHY. **00** = Speed is 10BASE-T 01 = Speed is 100BASE-TX 10 = Speed is 1000BASE-T 11 = Reserved
2	0	RO	**Reserved**
1	0	R/W RS	**Reset Control**. This bit controls whether or not the "Reset-Sticky" (RS) bits are reset (Register bit 28.1 = "1") to their default values, or remain in their current state (Register bit 28.1 = "0") when a MII (soft) reset is issued. **0** = MII issued reset will reset the "Reset-Sticky" bits to their default values 1 = VT6122 MII issued reset will not reset the "Reset-Sticky" bits to their default values
0	0	RO	**Reserved**

The VT6122 is by default configured to: 100BT advertised, full/half duplex advertised, autonegotiation enabled. These settings can be overridden by writing into the MII registers 0, 4, and 9.

Offset 1Dh: Delay Skew Status Register

Bit	Default	Type	Description
15	0	RO	**Reserved**
14:12	000	RO	**Pair A Delay Skew**. Skew in integral symbol times. These bits indicate the additional delay (measured in integral symbol times) added internally at the pair A receiver input to align received symbols at pair A with the received symbols at the other three pairs.
11	0	RO	**Reserved**
10:8	000	RO	**Pair B Delay Skew** [12]. Skew in integral symbol times. These bits indicate the additional delay (measured in integral symbol times) added internally at the pair B receiver input to align received symbols at pair B with the received symbols at the other three pairs.
7	0	RO	**Reserved**
6:4	000	RO	**Pair C Delay Skew.** Skew in integral symbol times. These bits indicate the additional delay (measured in integral symbol times) added internally at the pair C receiver input to align received symbols at pair C with the received symbols at the other three pairs.
3	0	RO	**Reserved**
2:0	000	RO	**Pair D Delay Skew.** Skew in integral symbol times. These bits indicate the additional delay (measured in integral symbol times) added internally at the pair D receiver input to align received symbols at pair D with the received symbols at the other three pairs.

Offset 1Eh: Reserved Register

Bit	Default	Type	Description
15:0	0h	RO	**Reserved**

Offset 1Fh: Reserved Register

Bit	Default	Type	Description
15:0	0h	RO	**Reserved**

[12] This value is valid only in 1000BASE-T mode.

FUNCTIONAL DESCRIPTION

The VT6122 Gigabit Ethernet controller is a CMOS VLSI designed for easy implementation of CSMA/CD IEEE 802.3u 10/100Mbps and 802.3z 1000Mbps Ethernet networks. Significant features include: PCI Plug and Play compatibility, 32/64 bit bus mastering, powerful buffer management and Adaptive Interrupt Control.

The VT6122 integrates the entire bus interface of PCI systems. The VT6122 also complies with PCI Specification v2.1, and v2.2.

Power Up Reset

The VT6122 implements a built-in power monitor for suspending power up; and maintains a clean internal Physical Layer clock and reset scheme. After the power on sequence is done, the VT6122 begins to load EEPROM and do chip initialization.

Host Bus Interface Control Logic

PCI Master Function

The VT6122 supports descriptor based communication list between hardware and software on both TX and RX; the DMA scheduler fetches the transmit and receive descriptors via PCI bus mastering to check if the buffers are free to store received packets and scheduled transmission requests.

Data Transfer between system buffers and internal FIFOs in VT6122 are executed by the DMA controller use the PCI bus bursting scheme and an advanced internal bus arbitration scheme to improve the bus utilization and service priorities

VT6122 also supports Look ahead scheduler to enqueue multiple transmit frames and back-to-back service received packets.

After receiving or transmitting processes is completed, VT6122 will write back the transfer and network status to the indexed descriptors to release the descriptors' ownership.

PCI Slave Function

VT6122 supports PCI slave register IO or memory mapped IO cycles for command and status registers, and supports PCI configuration cycles for plug & play BIOS.

Buffer Management

The VT6122 hardware controller and drivers communicate through two data structures:

- Control and status register (CSR)

- Descriptor entries and data buffers

During initialization, drivers create the structure of the Transmit and Receive descriptors in physical memory and decide base address for the Receive and Transmit descriptor rings. They are written to CSR18 (Desc_Base_Add_HI) for common Tx/Rx higher 32 bits address and CSR38 (RD_Base_LO) for Rx lower 32 bits address, CSR40(TD0_Base_LO), CSR44(TD1_Base_LO), CSR48(TD2_Base_LO), CSR4C(TD3_Base_LO) for TD queue 0~4 respectively. The number of entries contained in the descriptor rings and the buffer reserved in the physical memory for TD/RD are set up.

Each descriptor entry must occupy a contiguous area of memory. The Receive (Transmit) Descriptor DMA Register of CSR also keeps the content of current and next Receive (Transmit) Descriptor.

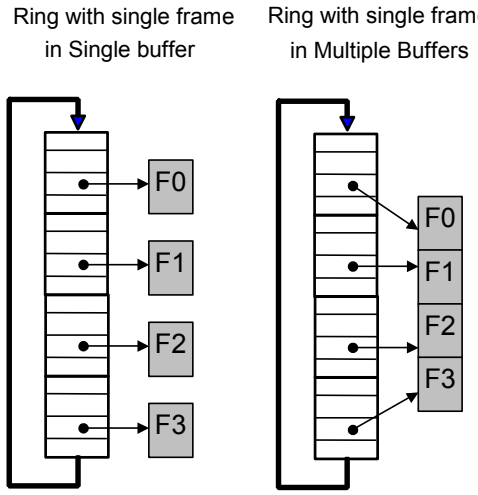


Figure 3. Buffer Structure

For reception, the controller receives data frames in Rx FIFO and updates the status information of Receive Descriptor DMA Register after reception is complete. It then proceeds to write back to descriptor in memory and bring data back using one DMA cycle.

For transmission, the controller starts the DMA cycle and brings the data from memory to Tx FIFO. Lately update the status information of Transmission Descriptor DMA Register after transmission complete and then proceed to write back to descriptor in memory using another DMA cycle.

Descriptors Information

Transmit Descriptor Command Block Format

Each command block defines a transmit packet with buffer segmentation

Transmit Descriptor List (TD) Ring

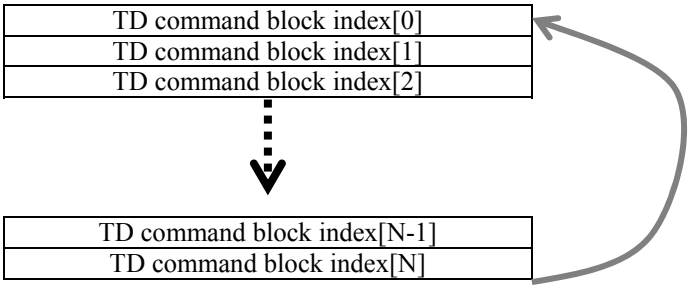


Table 12. Tx Descriptor Command Block Structure

TD+00	O		TX_Packet_Size[13:0]		TSR1	TSR0
TD+04	CMDZ	TCR1	TCR0		PQINF[15:0]	
TD+08	Tx_Data_Buffer_Address0.Lo					
TD+0c	Q		Tx_Buffer_Size0[13:0]		Tx_Data_Buffer_Address0.Hi	
TD+10	Tx_Data_Buffer_Address1.Lo					
TD+14	Tx_Buffer_Size1[13:0]				Tx_Data_Buffer_Address1.Hi	
TD+18	Tx_Data_Buffer_Address2.Lo					
TD+1c	Tx_Buffer_Size2[13:0]				Tx_Data_Buffer_Address2.Hi	
TD+20	Tx_Data_Buffer_Address3.Lo					
TD+24	Tx_Buffer_Size3[13:0]				Tx_Data_Buffer_Address3.Hi	
TD+28	Tx_Data_Buffer_Address4.Lo					
TD+2c	Tx_Buffer_Size4[13:0]				Tx_Data_Buffer_Address4.Hi	
TD+30	Tx_Data_Buffer_Address5.Lo					
TD+34	Tx_Buffer_Size5[13:0]				Tx_Data_Buffer_Address5.Hi	
TD+38	Tx_Data_Buffer_Address6.Lo					
TD+3c	Tx_Buffer_Size6[13:0]				Tx_Data_Buffer_Address6.Hi	

*Note.

1. Access principle : fetch 8DW each time, and more condition to fetch another 8 DW

2. TD must be allocated in 16-quadlets base address

3. We maintain the Hi data buffer address in separate register from {63:48}.

4 Each command block define a packet within 7 data segments

O		TxPktSize[13:0]/MTSR	TSR1	TSR0

Bit	Description	Updated by
31	**OWN.** Software maintained TD ownership information, WBTSR will be written back while support signal write back per packet option.	**DRV/HC**
30		**DRV/HC**
29-16	**TxPktSize[13:0].** TCP large send per segment packet size control fields. When write back. This fields are reserved for more status.	**DRV/HC**
15	**TERR.** Tx Error Status. TERR=ABT|GOWC|OWT|SHDN	**HC**
14	**FDX.** Current Transaction is serviced by Full Duplex mode	**HC**
13	**GMII.** Current Transaction is served by GMII mode else MII mode	**HC**
12	**LNKFL. "1" means packet serviced during link down.**	**HC**
11	**Reserved.**	**HC**
10	**SHDN.** "1" means shut down case, no guarantee for Tx ok	**HC**
9	**CRS.** Carrier Sense lost detection.	**HC**
8	**CDH.** Collision Heart beat detection failure in half duplex .	**HC**
7	**ABT.** Transmission Abort because of excessive Collision	**HC**
6	**OWT.** Jumbo Frame Tx abort.	**HC**
5	**OWC.** Out of window Collision.	**HC**
4	**COLS.** Collision seen in current good transmission OK status.	**HC**
3-0	**NCR[3:0].** Collision Counts in current good transmission OK status	**HC**

CMDZ	TCR1	TCR0	PQINF

Bit	Description	Updated by
31-28	**CMDZ[3:0].** CMDZ is used to determine how many segments are inside the command block (segment number =CMDZ-1)	DRV
27-26	**Reserved[1:0].**	DRV
25-24	**TCPLS_SOF,TCPLS_EOF.** 11: Normal Packet 10: Start of TCP Large Send Descriptor 00: Intermediate TD of a Large Packet 01: End of TCP Large Send Descriptor.	DRV
23	**TIC.** Request to issue interrupt while this packet status is transferred to TD wrk information ring	DRV
22	**PIC.** Priority interrupt request, make sure INTA# is issued over adaptive interrupt scheme	DRV
21	**VETAG.** Enable VLAN TAG, combine with HC control to insert VLAN tag	DRV
20	**IPCK.** Request IP checksum calculation.	DRV
19	**UDPCK.** Request UDP checksum calculation.	DRV
18	**TCPCK.** Request TCP checksum calculation.	DRV
17	**JMBO.** Indicated that a jumbo packet, to disconnect with burst frame, in Gmac side	DRV
16	**CRC.** Disable CRC generation in this packet	DRV
15-13	**Pri[2:0].** 802.1p priority bits	DRV
12	**CFI,** Reserved control bit	DRV
11-0	**VLAN_ID[11:0].** 802.1q Virtual LAN Identifier	DRV

Receive Descriptor Command Block Format

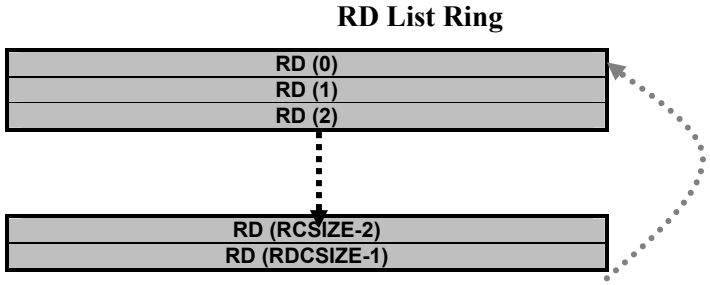


Table 13. Receive Descriptor Formwt (RD)

RDE0	**O**		**RMBC[13:0]**										**RSR1**		**RSR0**
RDE1	***IPKT***								***CSM***				**PQTAG**		
RDE2	**RX_DATA_BUFFER_ADDRESS.Lo**														
RDE3	**I***			**RX_Buffer_Size[13:0]**									**RX_DATA_BUFFER_ADDRESS.Hi**		

***I = interrupt control enable**

Offset 03h ~ 00h: RD Command Block Header 0 Field

O		RMBC [13:0]	RSR1	RSR0

Bit	Description	Updated by
31	**OWN.** Software maintained RD ownership information, 1= DESC owned by NIC 0= owned by host,	DRV/HC
30	**SHDN. Shut down case**	HC
29-16	**RMBC[13:0].** Received Packet Byte Count.	HC
15	**RXOK.** Packet received ok.	HC
14	**PFT.** Perfect filtering address match, check the PQTAG encode to see if interesting packet hit	HC
13	**MAR.** NIC accept multicast address packet	HC
12	**BAR.** NIC accept broadcast address packet	HC
11	**PHY.** NIC accept unicast address packet	HC
10	**VTAG.** 802.1p/802.1q tagging packet indicator	HC
9-8	**STP,EDP.** STP : packet start, in Desc ring structure 00 : Single packet in Single RD 10 : Start of Chained Packet 11 : Intermediate segments of chained packet 01 : End of Chained Packet	HC
7	**DETAG.** HC de-tag indicator.	HC
6	**SNTAG.** Received a SNAP packet with tag.	HC
5	**RXER.** PCS symbol error	HC
4	**RLE.** Receive length error indication.	HC
3	**CE.** Receive check sum error indication.	HC
2	**FAE.** Receive frame alignment error indication.	HC
1	**CRC.** Receive CRC error indication.	HC
0	**VIDM.** VID filtering miss	HC

Offset 07h ~ 04h: RD Command Block Header 1 Status Field

IPKT	CSM	PQTAG

Bit	Description	Updated by
31-30	**Reserved.**	**HC**
29-24	**IPTn.** Indexed 64 bit perfect and interesting packet filtering - Normally we use CAM 32 ~ 63 as interesting packet filtering	**HC**
23	**Reserved.**	**HC**
22	**IPOK.** NIC IP checksum validation OK.	**HC**
21	**TUPOK.** NIC TCP/UDP checksum validation OK.	**HC**
20	**FRAG.** Fragment IP datagram	**HC**
19	**CKSMZO:** received packet with zero value on UDP checksum field .	**HC**
18	**IPKT.** NIC received a IP packet.	**HC**
17	**TPKT.** NIC received a TCP packet.	**HC**
16	**UPKT.** NIC received a UDP packet.	**HC**
15-0	**PQTAG.** The 802.1p/802.1q tag data of received packet, if any.	**HC**

FIFO and Control Logic

The VT6122 incorporates two independent FIFOs for transmission (16K bytes) or receive (48K bytes) data buffering from the system interface to the network interface, providing temporary storage of data, to free host system from the real-time demands on the network.

The VT6122 Transmit FIFO controller has advanced adaptive traffic control mechanism to maintain a back-to-back sned at wire speed.

The VT6122 has enhanced Receive FIFO management logic to handle multiple received data packets transfer to system data buffer. This ability can reduce the packets losing due to PCI bus mastering arbitration latency.

Media Type and Auto-Negotiation

The VT6122 supports 10Base-T / 100Base-T / 1000Base-T.

The 802.3 2002 Auto-Negotiation defines automatic negotiation of signaling rate and duplex mode between two ends of a twisted pair link segment. The VT6122 supports Auto-Negotiation defined Priority Resolution Table fetched from the integrated PHY to decide current operating mode of the media port.

The VT6122 supports media port selected in different ways depending open the state of internal configuration.

Auto-Negotiated/Force mode.

Through Auto-Negotiation, the PHY attempts to negotiate a 10/100/1000 Base-T link with a remote adapter. After the negotiation process is completed, the VT6122 can decide if a link is up and the speed rate and duplex through polling the PHY's Auto-Negotiation registers.

Also, the VT6122 also can be programmed to a desired operating speed 10/100/1000Gbps and duplex mode (FDX or HDX) through forced operation.

CAM Based Perfect filtering

The address recognition logic of VT6122 controller uses Content Address Memory (CAM) technology to support unicast, multicast and interesting packets perfect filtering and VID perfect filtering for VLAN supporting

Programming CAM.

The VT6122 driver initializes CAM by enabling CAM read/write function, CAMEN= 1

- set CAM entry address, (CAMADD)
- set CAM entry data
- Address_CAM: 0x10 ~ 0x15, 48 bits
- VID_CAM : 0x10 ~ 0x11, 12 bits
- set CAMWR.
- wait CAMWR self clear
- execute next CAM entry programming

Read CAM

The VT6122 driver download CAM contents by

- enable CAM read/write function, CAMEN= 1
- set CAM entry address (CAMADD)
- set CAMRD.
- wait CAMRD self clear.
- read CAM content from data port
  Address_CAM : 0x10 ~ 0x15, 48 bits
  VID_CAM: 0x10 ~ 0x11, 12 bits

Unicast/Multicast Perfect Filtering.

Program Address_CAM with accepted Ethernet address.

Turn on the CAMMASK bits to enable related Address_CAM entries.

Turn on AM: incoming multicast packets will be filtered with perfect address.

Turn on AP: all incoming packets will be filtered by comparing with those active entries (CMMASK bits enabled) defined in Address_CAM.

If the number of multicast address is larger than 64, the multicast hash tables can be used also.
CAM content won't be cleared by any types of reset. We can only control the CAMMASK to handle the active entries.

Interesting Packet Perfect Filtering.

Interesting packets are a group of packets with specified Multicast Address. The VT6122 provides max 32 interesting packets filtering capability. The hits index will be stored and write-back to RD status.

The operation is as follows:
- Program the interesting packet address into Address_CAM.
- For each incoming packet, check the RD.IPKT field to see which interesting packet received.

Checksum Offload

The VT6122 provides hardware based TCP/IP, UDP/IP checksum calculation and validation. On Transmission, the Host requests TCP/IP checksum offloading by setting the control bit in the transmit descriptor (TD) header control field. On reception, when the checksum offload enable bit is set, every packet is parsed for the presence of IP, TCP, and UDP headers. For any of those found, checksum logic will calculate and compare with those related fields in the packet. Any mismatches will be flagged as checksum errors and the status is kept at write back status field and is transferred to the host by normal packet reception write back flow.
VT6122 checksum offload feature supports Ipv4 only, packets of other IP versions will be ignored.
IP forms are EtherType = 0800h, IEEE 802.2 and SNAP.
Fragmented IP datagrams are not supported.

IEEE 802.1q Compliant VLANs

VLAN

The VT6122 supports IEEE 802.1q Virtual Local Area Network (VLAN). In a VLAN environment, the controller will respond to range of 64 individual addresses, allowing multiple VLAN support.

IEEE 802.1q VLANs

802.1q frames have 4 extra bytes over normal 802.3 frame format. Two of the 4 bytes contain a special type (TPID) and the other two bytes contain 12 bit VLAN ID number, 3 bits of priority and a "token Ring encapsulation" bit. The VT6122 adapter will take an oversized frame on a 802.1q packet if it is larger than MaxPktSize+4.

With frame tagging, each VT6122 can support up to 64 IP address assignments on a single network connection, allowing servers to be accessed from systems in multiple IP subnets without traversing routers. It also allows users to define multiple application VLANs to partition traffic for performance and security purposes.

In summary,

The VT6122 support Multiple Virtual LAN (VLAN)

Long frame support (1518 + 4) bytes

- VLAN tag insertion for transmit packets
- VLAN tag detection and removal for receive packets.
- VLAN status could be written back to the Receive Descriptor.

IEEE 802.1p Priority Transmit

To Meet current Multi-Media application and maintain the Quality Of Service,(QoS), VT6122 supports IEEE 802.1p and provides 4 levels of priority. The priority DMA scheduler maintains flexible queuing usage depends on driver's setting. The VT6122 hardware and software maintain 4 TD queues in advanced priority DMA scheduler, and also provide non-blocking mode for high performance application requirement.

Flow Control

The VT6122 supports half duplex Jam based and IEEE802.3x flow control scheme while in full duplex .

When VT6122 detects if the system is busy and receive buffers or the internal FIFO are running up:

In half duplex mode, MAC will send jam pattern automatically, when addressed packets coming to stop the transmission from source station.

In full duplex mode, VT6122 will generate PAUSE control frame to inform the source station to stop transmission for specified period of time defined in the PAUSE frame. After the busy condition is clear, VT6122 will send another PAUSE control frame with pause_time(0000h) to inform the source station of getting ready to receive packets.

VT6122 also implements detection logic to filter coming pause control frame, when a valid PAUSE control frame is detected, VT6122 will enter backoff state after current transmission completed and wait for the specified period of time defined in the received PAUSE frame. VT6122 will RE-transmit other packets in transmit queue after receiving a new pause frame with pause_time(-0000h) or when the pause timer is expired. Also, the IEEE802.3x flow control capability is the negotiated results from N-way and can be optionally disabled.

Statistics

The VT6122 provides network traffic statistics to ease the network management.

1.	RxAllPkts	The total number of packets (including **bad packets**, broadcast packets, and multicast packets) received.
2.	RxOkPkts	The number of incoming frames that are successfully received.
3.	TxOkPkts	The count of the number of frames that are successfully transmitted.
4.	RxErrorPkts	Frames Lost Due to Receive Errors is a count of the number of frames that should have been received (the DA matched) but experienced a receive FIFO overrun error. Only includes overruns that become apparent to the host system, and does not include frames that are completely ignored due to a completely full rxfifo at the beginning of frame reception
5.	RxRuntOkPkt	Packet size < 64 and well formed
6.	RxRuntErrPkt	It counts both runts and noise hits. packet size < 64 and error.
7.	Rx64Pkts	Counting the incoming packet byte include 802.1p/q tag regardless of whether the tag removing or not.. packet size = 64
8.	Tx64Pkts	Number of transmitted packet with 64octets.
9.	Rx65To127Pkts	Number of accepted packets with byte count, 65 =< size <= 127
10.	Tx65To127Pkts	Number of transmitted packet with byte count, 65 =< size <= 127
11.	Rx128To255Pkts	Number of accepted packets with byte count. 128 =< size <= 255
12.	Tx128To255Pkts	Number of transmitted packets with byte count. 128 =< size <= 255
13.	Rx256To511Pkts	Number of accepted packets with byte count, 256 =< size <= 511
14.	Tx256To511Pkts	Number of transmitted packets with byte count, 256 =< size <= 511
15.	Rx512To1023Pkts	Number of accepted packets with byte count, 512 =< size <= 1023
16.	Tx512To1023Pkts	Number of transmitted packets with byte count, 512 =< size <= 1023
17.	Rx1024To1518Pkts	Number of accepted packets with byte count, 1024 =< size <= 1518
18.	Tx1024To1518Pkts	Number of transmitted packets with byte count, 1024 =< size <= 1518
19.	TxEtherCollisions	The total number of collision on Ethernet segment
20.	RxPktCRCE	Number of incoming packet with CRC error
21.	RxJumboPkts	Number of accepted Jumbo Packets
22.	TxJumboPkts	Number of transmitted Jumbo Packet
23.	RxMacControl Frames	The number or MAC control PAUSE frames, and only PAUSE frames, received successfully.
24.	TxMacControl Frames	The count of MAC control frames transmitted. Not include the frame transmitted by host.
25.	RxPktFAE	Number of accepted packet with Frame Alignment Error
26.	RxLongOkPkt	Number of accepted packets with byte counted larger than 1518
27.	RxLongPktErrPkt	Number of incoming packet with error and packet byte count larger than 1518
28.	TXSQEErrors	Number of SQE errors
29.	RxNobuf	Number of Receive No buffer events.
30.	RxSymbolErrors	Number of symbol error
31.	InRangeLenth Errors	Number of accepted packet with length error. Length range 64 <= PktLen <= 1518
32.	LateCollisions	Late Collisions is a count of the number of times that a collision has been detected later than 1 slot time into the transmitted frame

MIB Read Access.

Toggle MIBCR.MIBCLR to clear all mib counter after HardReset/SoftReset.
Clear MIBCR.MIBFRZ to start mib count.
Select MIB indication thresh by MIBCR.MIBHI.
As CNTI occurs, toggle MIBCR.MIBINI to make read pointer returned to zero, then read all MIB counters by 32 continuous IOR (MEMR) MIBDATA port.
All MIB counters will be auto-cleared.
After all MIB counter read out, clear ISR
If any uncertain event breaks MIB collection routine (32 continuous read), MIBCR.MIBINI can be used to reset MIB read pointer to zero.

EEPROM Interface

EEPROM Direct Programming

The VT6122 features an easy way to program an external EEPROM in-system. After the RESET is de-asserted and if the upper byte of 0FH on EEPROM is not 73H, the CHIPGSR.EEPR bit will not be set to indicate that the current EEPROM has not been programmed yet. This will allow the VT6122 to enter Direct Programming mode if EELOAD is also set. In this mode the user can directly control the EEPROM interface signals by writing to the EECSR Port and the value on the EECS, ESK and EDI bits will be driven onto the EECS, SK(MD2), and DI(MD1) outputs respectively. These outputs will be latched so the user can generate a clock on SK by repetitively writing 1 then 0 to the appropriate bit. This can be used to generate the EEPROM signals as per the 93C46 data sheet.

To read the EEPROM data, users have to generate EEPROM interface signals into EECS, DI and SK as described above and in the mean time read the data from DO(MD0) input via pin SD0. Reading Data Transfer Port during programming will not affect the latched data on EECS, SK, and DI outputs. When the EEPROM has been programmed and verified (remember to program the upper byte of 0EH & 0FH with 73H), the user must give VT6122 a power-on reset to return to normal operation and to read in the new data.

The Direct Programming mode is mainly used for production to program every bit of the EEPROM. Once the upper byte of 0EH has been programmed with 073H and a power-on reset has been performed, there is no way to change the contents of EEPROM except Configuration Registers A, B, and C, which will be discussed in the following paragraph. For more information, refer to EECSR.

EEPROM Embedded Programming

Besides direct programming of EEPROM, VT6122 also provide embedded EEPROM programming engine. Through embedding EEPROM programming routines, driver can read/write each entry of EEPROM by a series simple IOR (MEMR) IOW (MEMW).

EEPROM Contents

VT6122 supports 93c06, 93c46, 93c56 serial ROM, and the on board serial ROM is to store Ethernet ID, Sub vendor ID, and some chip configurations (list in Table below).

Table 14. Chip Configuration EEPROM Contents

Offset ID	Bit[15:8]	Bit[7:0]
00 h	Ether ID[15:8]	Ether ID[7:0]
01 h	Ether ID[31:24]	Ether ID[23:16]
02 h	Ether ID[47:40]	Ether ID[39:32]
03 h	SW-DATA	(G)MII PHYID
04 h	SUB_SID[15:0]	SUB_SID[7:0]
05 h	SUB_VID[15:0]	SUB_VID[7:0]
06 h	Reserve	Reserve
07 h	Reserve	Reserve
08 h	Reserve	PMCC
09 h	Reserve	Reserve
0A h	Reserve	Reserve
0B h	MAX_LAT	MIN_GNT
0C h	DCFG1	DCFG0
0D h	CFG_B	CFG_A
0E h	CDG_D	CFG_C
0F h	checksum	(73 h)

Offset ID	Description
0-2	**Ethernet global ID**
3	**Reserve for future use, must be 00h always**
4	**PCI configuration space sub system ID**
5	**PCI configuration space sub vender ID**
6	**Reserve for future use, must be 00h always**
7	**Reserve for future use, must be 00h always**
8	**PCI power management capability setting** **[15:8] reserve for future use, must be (00 h) always** **PMCC : power management capability control** **Bit-0: D0_En … D0 state capable** **Bit-1: D1_En … D1 state capable** **Bit-2: D2_En … D2 state capable** **Bit-3: D3h_En … D3 hot state capable** **Bit-4: D3c_En … D3 Aux power state capable** **Bit-5: D1_Dis … disable D1 state support** **Bit-6: D2_Dis … disable D2 state support** **Bit-7: DSI … DSI in PMU register, "0" always**
9	**Reserve for future use, must be (00 h) always**
A	**Reserve for future use, must be (00 h) always**
B	**PCI configuration space minimum grant, maximum latency setting**
C	**Internal CSR Bus configuration setting**
D - E	**Internal CSR Chip configuration setting**
F	**Checksum and EEPROM programmed indicator**

Power Management

The VT6122 is compliant to ACPI V1.0, PCI Power Management V1.1 and Network device class power management V1.0a. It meets PC97/PC98/PC99/PC2001 and net PC requirements. When the system enters power down mode, four wake-up events are supported in VT6122 and can wake up the system via PME# to restore to running state to process normal jobs when wake up events are detected.

Wake On LAN

The VT6122 can be configured to support remote wake up by defined wake up events in every PCI PMU defined power states via PME# indication. Also a Magic packet scheme

Wake up at PCI power abnormal shut down or AC power loss by remote Wake On LAN management station.

Wake Up Events

- **Link Status Change**: If this link state have changed connect or disconnected , PME# will be generated when link state change.
- **Magic Packet:** When VT6122 is set to magic packet mode, it require that a received packet qualify as a Magic Packet
- **Magic Packet Pattern:** The Magic packet pattern 6 FFh byte + SA duplication 16 times destination address of received magic packet matches, meanwhile Magic register (RxA0[5]) set enable, VT6122 will received this packed.
- **Unicast Physical Address Match:** When VT6122 is set to unicast mode, it require that a received packet qualify as a unique individual address and unicast register bit (RxA0[5]) set enable, VT6122 will received this packed.
- **MS Defined Pattern Match:** When the stations shutdown after operation system is loaded, the IP address, station name or other defined value are set by the drivers to VT6122 define 8 (or 16) sets of interesting pattern match.

Power States

Table 15. Power States

VT6122 Device state	Condition	L_PCI mA	I_AUX mA	Action from Function
D0	PCI=66, MAC=125M Tx,Rx Active			Full function
D1,D2	PCI=66M, MAC=25M PCI bus transaction IDLE			Wake up event detection
D3 hot	PCICLK IDLE, MAC=25M TX off, RX on			Wake up event detection
D3 cold	PCI power off, MAC=25M Tx off, RX on			Wake event detection

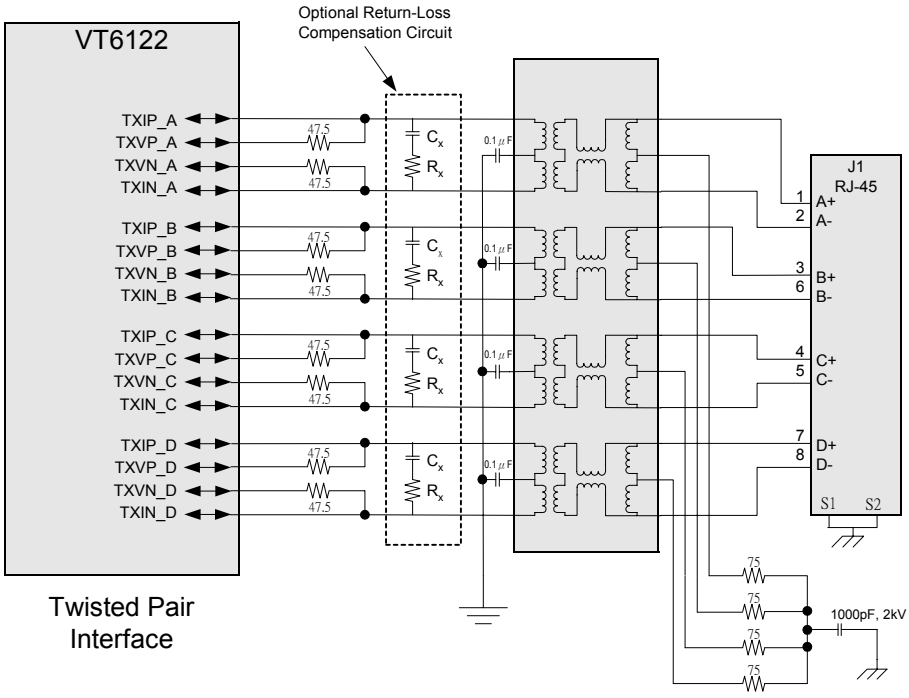
PHY

The VT6122 transceiver is based on a highly robust DSP Data Pump architecture with a triple speed capable Analog Front End (AFE). At the systems level, the following components are required to interface to the VT6122:

- A single reference clock (either 25MHz or 250MHz), or an optional single 25MHz crystal
- Up to two fixed power supplies, 3.3V and 1.5V, or only 3.3V with use of the device's on-chip switching voltage regulator)
- A 1:1 quad transformer module[13]
- Power supply decoupling capacitors
- Eight 47.5 Ω Termination resistors

Twisted Pair Interface (TPI)

- Connects the VT6122 integrated PHY port's four dual-duplex channels to an external 1:1 transformer module.
- The integrated PHY implements an internal hybrid, which minimizes the number of external passive components and easily interfaces to several, readily available, quad transformer modules to support all three operating modes.



Operation Mode Presetting

Optional configuration pins, MODE (10, 100, and 1000), FRCDPLX, and ANEGDIS, provide an alternative, direct method for presetting the operating mode (speed and duplex) of the integrated PHY port without the need for a dedicated station manager.

[13]For PICMG 2.16 applications, the transformer can be removed. See *PICMG 2.16 Applications Note* for more information.

System Clock Interface

Allows either a single 25MHz reference clock or an optional reference crystal (used with the on-chip oscillator) to be used as the reference clock for the device.

The SCI is a three-pin interface comprised of the LED3(OSC_BYPASS), XTAL1/REFCLK and XTAL2 pins. LED3 is a bidirectional pin that is sampled during power-up or system reset sequences. When the on-chip oscillator is bypassed, a 25MHz clock with a 100ppm frequency offset has to be supplied from an external clock source.

A 250MHz clock can also be used, when both the on-chip oscillator and on-chip PLL are bypassed (attach pullup resistors to the LED3 and MA0 pins during power-up or system reset).

Test Mode Interface (TMI)

- Enables IC manufacturing test and standard board-level testing through an industry standard JTAG 1149.1 Boundary Scan controller.
- Facilitates the operation of several innovative analog and digital Built-in-Self-Test functions, which simplify and improve manufacturing test coverage, leading to reduced component and systems costs.

Analog Front End (AFE)

The analog front end, or "AFE", performs the following functions in each operating mode:

- Receive and transmit signal separation (via on-chip hybrid circuitry)
- Transmit wave filtering and shaping (PMA Transmit Filter and AFE TX DAC)
- Automatic gain control (VGA)
- Receive signal quantization (ADC)
- Digital timing recovery (ADC and VGA, in concert with DSP Data Pump Core)
- Link pulse detection

In the receive data path, digital words quantized by the PHY port's four ADCs are supplied to the PMA (Physical Media Attachment) for further processing by the various DSP Data Pump elements (Adaptive equalization, Echo cancellation, NEXT and FEXT cancellation, trellis decoder, and the digital timing recovery loop).

On the transmit data path, the digital transmit filters in the PMA provide digital transmit words in 3-bit PAM5 (1000BASE-T), MLT-3 (100BASE-TX), or Manchester-encoded format to the triple speed, pulse-shaping transmit DACs.

The AFE also includes an analog PLL, which generates all internal and externally-sourced clocks from either a 25MHz or 250Hz reference clock (or a reference crystal, used with the on-chip oscillator).

DSP Data Pump Core (PMA)

Due to a robust, low-power DSP architecture, the VT6122 eases interoperability concerns by maintaining error-free operation in the presense of extreme noise and interference and in substandard cabling environments. It also supports link partner frequency offset tolerances well outside the Ethernet specifications (typically 450ppm of local and link partner frequency offset tolerances).

The primary Receive functions performed within the DSP Data Pump include:

- Echo cancellation
- Crosstalk cancellation (near and far end)
- Baseline wander correction and cancellation
- Adaptive receive equalization
- Receive signal slicing
- Digital timing recovery
- Cable pair skew compensation
- Trellis decoding (or forward error correction)

Other functions performed by the DSP core include:

- Automatic pair swap detection and correction
- Automatic cable pair polarity compensation
- Automatic MDI crossover for all three speeds

The primary transmit function implemented by the DSP core is:

- Transmit pulse shaping

Physical Coding Sublayer (PCS)

The PCS is responsible for controlling all transmit and receive data interchanges with MACs, the PCS transfers data to and from the MAC at various word widths, in conjunction with several MAC interface control signals.

For example, in 1000BASE-T mode, the PCS receive path includes three primary functions:

- Trellis decoding
- Symbol descrambling
- 4D-PAM5 symbol demapping

These elements serve together to:

- Convert PAM-5 symbols from the DSP core into 8-bit receive data symbols for transmission to the MAC
- Generate the associated receive data control and status signals for use by the MAC

In 1000BASE-T mode, the PCS transmit path includes the following functions:

- Trellis encoding
- Symbol scrambling
- 4D-PAM5 symbol encoding

From a functional perspective, these elements serve together to:

- Convert transmit data words from the MAC to PAM-5 symbols, which are sent to the transmit filters and DACs in the DSP core and AFE, respectively

Optional Fixed Power Supply Regulator

The VT6122 can optionally be powered from a single 3.3V power supply when utilizing the device's on-chip switching regulator circuit to produce the 1.5V core power supply voltage. To generate the required 1.5V core voltage for the device, VT6122 integrates an efficient "Buck Converter" type switching regulator. The switching regulator requires only two off-chip components –an inductor and a capacitor.

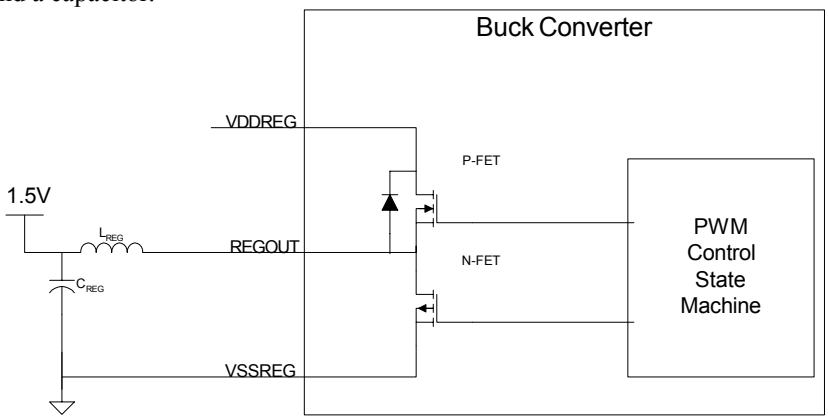


Figure 4. Buck Converter Architectural Schematic

External Component Requirements

Component	Min	Typ	Max	Unit	Description
C_{REG}		20		µF	
L_{REG}		3.3		µH	Critical requirements are low series resistance (<0.2Ω) and high dc current rating (>600mA)

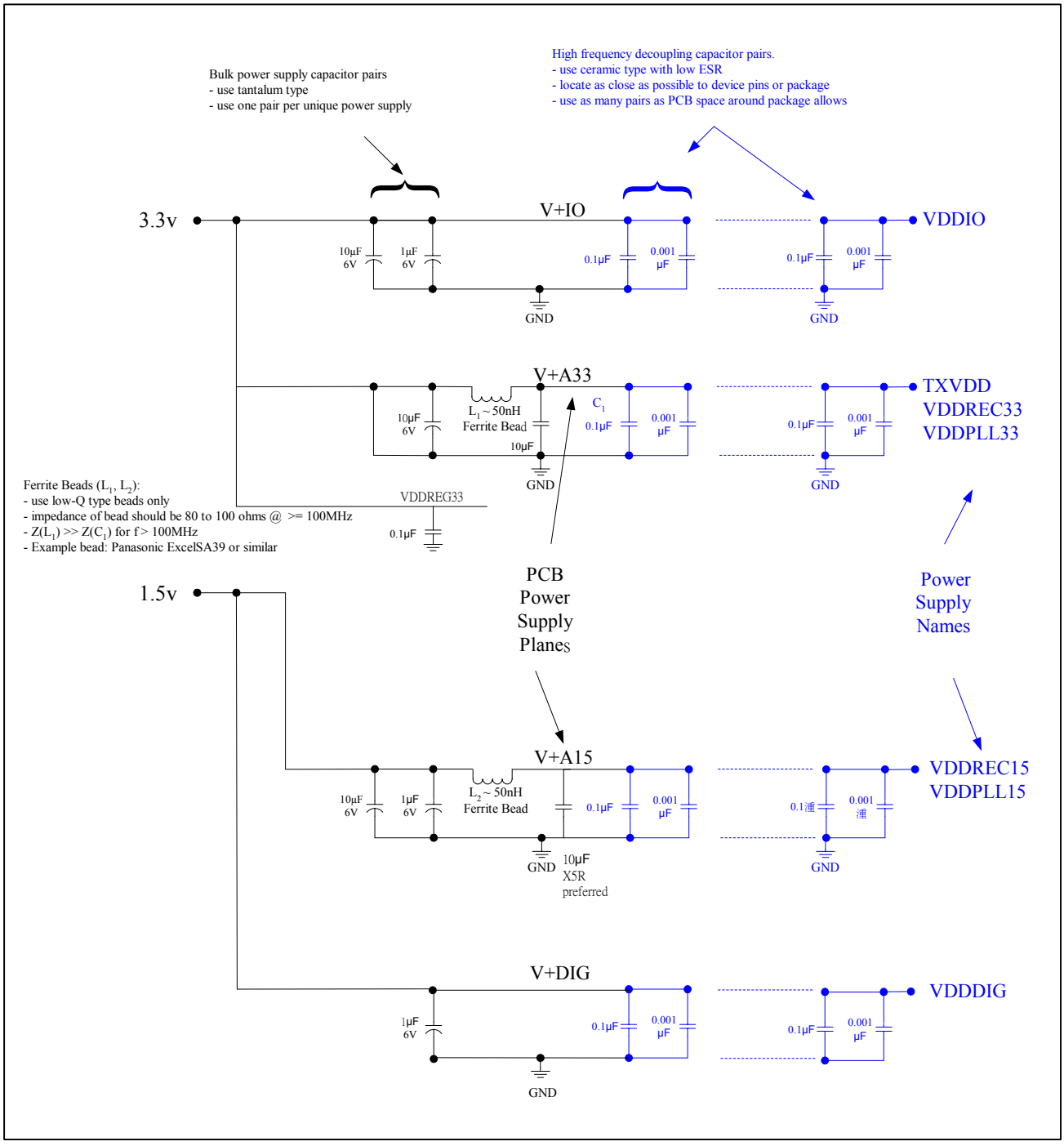


Figure 5. 3.3V and 1.5V Power Supply Configuration

Parallel LED interface

5 status LEDs with 4 programmable modes to communicate its operating conditions (activity, duplex, lnk1000, lnk100, lnk10). In LOM (Lan On Motherboard) application, the most popular configuration is using one RJ-45 jack with 2 glued LEDs. One of them is built with single light and the other one is built with dual lights. As following diagrams show:

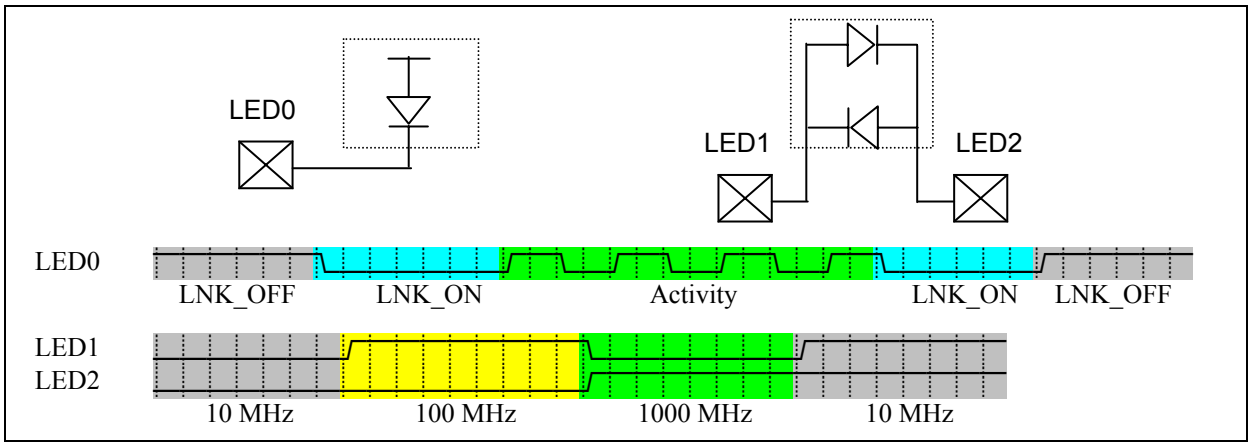


Figure 6. Case 1

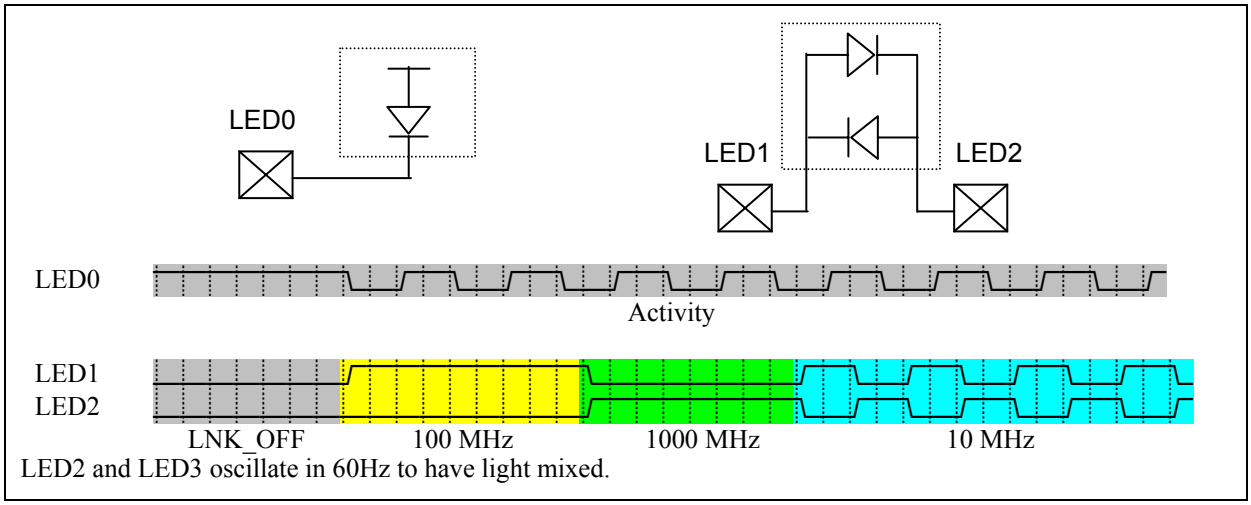


Figure 7. Case 2

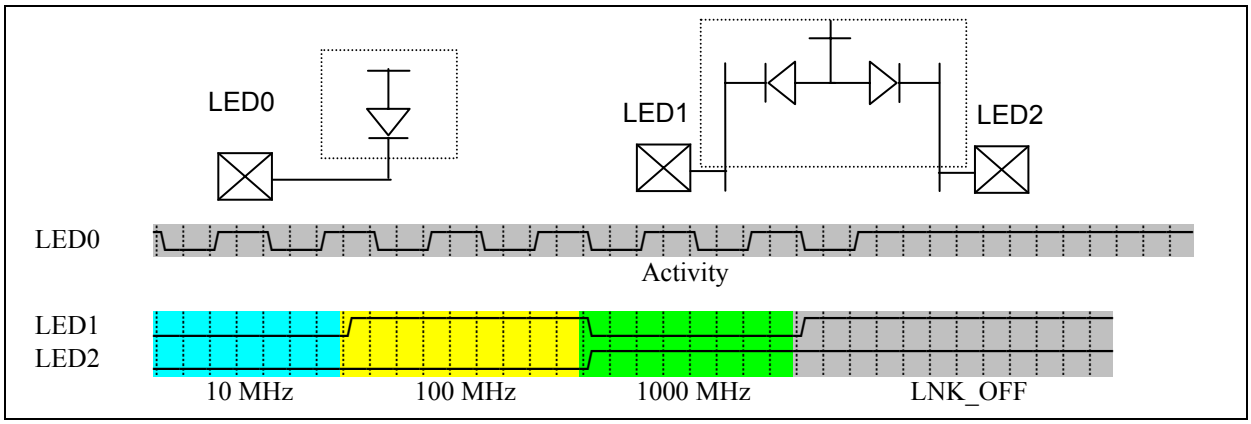


Figure 8. Case 3

LED Control Spec

Table 16. LED Select

LEDS1,LEDS0	LED0	LED1	LED2	LED3	LED4	Note
0,0	Activity	Duplex	LNK10	LNK100	LNK1000	All High active
0,1 (Default)	CASE_1			0	0	LED 0 Low active LED1, LED2 see CASE_1
1,0	CASE_2			0	0	LED 0 Low active LED1, LED2 see CASE_2
1,1	CASE_3			0	0	LED 0 Low active LED1, LED2 see CASE_3

LED select bits are in CFG_A register Rx78[5:4]
0: For Nothing

The VT6122 includes LED output signals in parallel via directly driving LED status output pins. When enabled by MII Register bit 27.3, all LED outputs are pulsed at 5KHz with a 20% duty cycle for low-power operation.

Table 17. PLI Bit Definitions

LED Status Bit	Active State (asserted high)	Inactive State (asserted low)
Duplex	Link is operating in full-duplex mode	Link is operating in half-duplex mode. Collision LED function is turned on, causing this LED to visibly blink at a 5Hz rate when collisions occur.
Link1000	Link established at 1Gbps	Link NOT established at 1Gbps
Link100	Link established at 100Mbps	Link NOT established at 100Mbps
Link10	Link established at 10Mbps	Link NOT established at 10Mbps
Activity[14]	Link is established and Transmit or Receive activity detected	Transmit or Receive activity NOT detected

[14]Activity can be programmed to be steady state or blinking.

Test Mode Interface (JTAG)

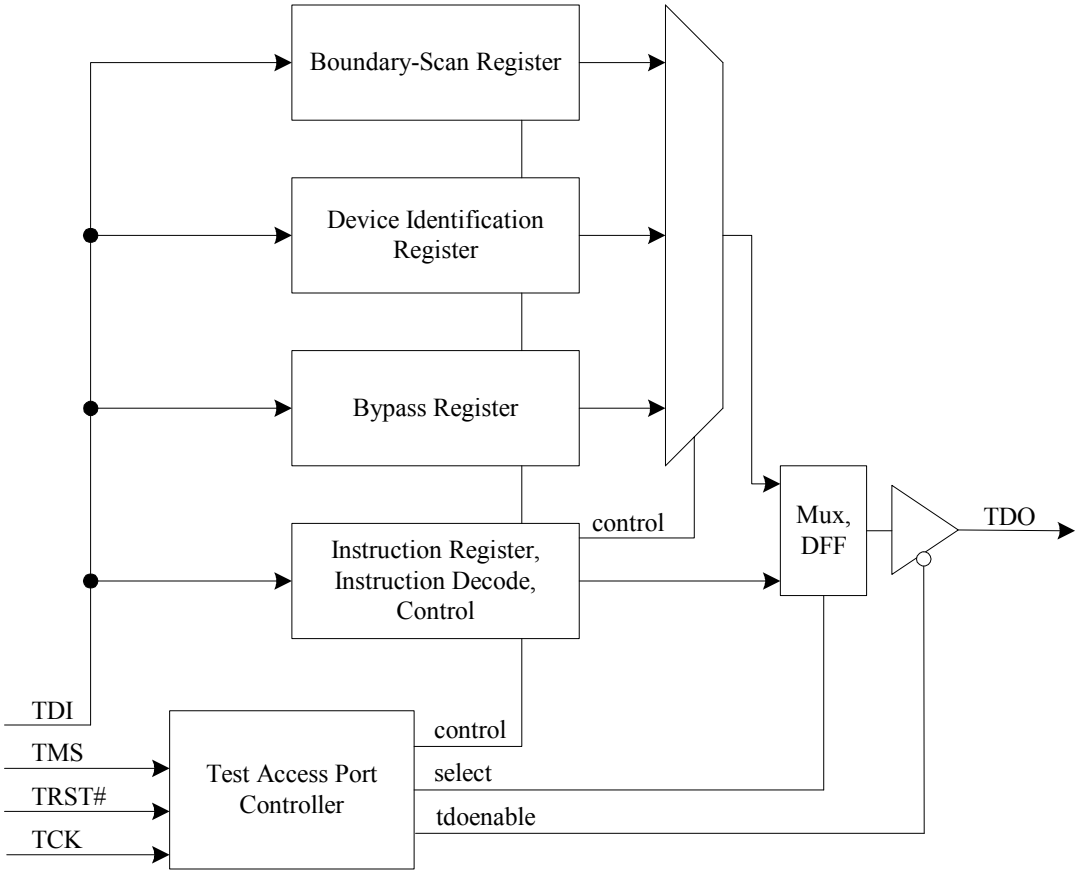
The VT6122 supports the Test Access Port and Boundary Scan Architecture IEEE 1149.1 standards. The device includes an IEEE 1149.1 conformant test interface, often referred to as a "JTAG TAP Interface". IEEE 1149.1 defines test logic to provide standardized test methodologies for:

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate.
- testing the integrated circuit itself during IC and systems manufacture
- observing or modifying circuit activity during the component's normal operation.

The JTAG Test interface logic on the VT6122, accessed through a Test Access Port (TAP) interface, consists of a boundary- scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal RST#. Refer to the IEEE 1149.1 specification for additional information about these pins.

The following figure diagrams the TAP and Boundary Scan Architecture.

Figure 9. Test Access Port and Boundary Scan Architecture



The VT6122 also includes the optional Device Identification Register, shown in the following table, which allows the manufacturer, part number and version number of the device to be determined through the TAP Controller. See Chapter 11 of the IEEE 1149.1-1990 specifications for more details. Also, note that some of the information in the identification register is duplicated in the IEEE-specified bit fields in MII Register 3 (PHY Identifier Register #2).

Table 18. JTAG Device Identification Register Description

Description	Device Version Number (or Revision Code)	Part Number (or Model Number)	Manufacturer Identity	LSB
Bit Field	31 – 28	27 - 12	11 – 1	0
Binary Value	4'h1	16'h8311 (32-bit option) 16'h8301 (64-bit option)	00110011000	1

The JTAG TAP port's AC timing requirements can be found in Table 26.

Supported Instructions and Instruction Codes

After a TAP reset, the Device Identification Register is serially connected between TDI and TDO by default. The TAP Instruction Register is loaded either from a shift register (when a new instruction is shifted in), or, if there is no new instruction in the shift register, a hard-wired default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

The VT6122 supports the instruction codes listed in the following table and described below.

Table 19. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	Specification
EXTEST	000	Boundary-Scan Register	75	Mandatory IEEE 1149.1
SAMPLE/PRELOAD	001	Boundary-Scan Register	75	Mandatory IEEE 1149.1
IDCODE	110	Device Identification Register	32	Optional IEEE 1149.1
CLAMP	010	Bypass Register	1	Optional IEEE 1149.1
HIGHZ	011	Bypass Register	1	Optional IEEE 1149.1
BYPASS	111	Bypass Register	1	Mandatory IEEE 1149.1
Reserved	100			

EXTEST
The mandatory EXTEST instruction allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.[15]

SAMPLE/PRELOAD
The mandatory SAMPLE/PRELOAD instruction allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE
The optional IDCODE instruction provides the version number (bits 31:28), part number (bits 27:12), and manufacturer identity (bits 11:1) to be serially read from the VT6122. See Table 18 for instructions on the values specific to the VT6122.

CLAMP
The optional CLAMP instruction allows the state of the signals driven from the component pins to be determined from the Boundary-Scan Register while the Bypass Register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins will not change.[16]

HIGHZ
The optional HIGHZ instruction places the component in a state in which *all* of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.

[15] Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.
[16] Following the use of this instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return to normal (i.e., non-test) operation.

BYPASS

The Bypass Register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

Boundary-Scan Register Cell Order

All inputs and outputs are observed in the Boundary-Scan Register cells. All outputs are additionally driven by the contents of Boundary-Scan Register cells. Bidirectional pins have all three related Boundary-Scan Register cells: the input, the output, and the control.

Port ordering from TDI to TDO is listed in the following table.

Table 20. VT6122 Port Ordering from TDI to TDO

No	Port	Type	No	Port	Type
1	LED4 (IN)	Observe	35	REDUNDANT	Observe
2	LED4 (OUT)	Control/Observe	36	REDUNDANT	Control/Observe
3	LED4 (CTRL)	Control/Observe	37	REDUNDANT	Control/Observe
4	LED3 (IN)	Observe	38	REDUNDANT	Observe
5	LED3 (OUT)	Control/Observe	39	REDUNDANT	Control/Observe
6	LED3 (CTRL)	Control/Observe	40	REDUNDANT	Control/Observe
7	LED2 (IN)	Observe	41	MD0 (IN)	Observe
8	LED2 (OUT)	Control/Observe	42	MD0 (OUT)	Control/Observe
9	LED2 (CTRL)	Control/Observe	43	MD0 (CTRL)	Control/Observe
10	LED1 (IN)	Observe	44	MD1 (IN)	Observe
11	LED1 (OUT)	Control/Observe	45	MD1 (OUT)	Control/Observe
12	LED1 (CTRL)	Control/Observe	46	MD1 (CTRL)	Control/Observe
13	LED0 (IN)	Observe	47	MD2 (IN)	Observe
14	LED0 (OUT)	Control/Observe	48	MD2 (OUT)	Control/Observe
15	LED0 (CTRL)	Control/Observe	49	MD2 (CTRL)	Control/Observe
16	GPIO (IN)	Observe	50	REDUNDANT	Observe
17	GPIO (OUT)	Control/Observe	51	REDUNDANT	Control/Observe
18	GPIO (CTRL)	Control/Observe	52	REDUNDANT	Control/Observe
19	PVDET (IN)	Observe	53	MD4 (IN)	Observe
20	TESTM1 (IN)	Observe	54	MD4 (OUT)	Control/Observe
21	TESTM1 (OUT)	Control/Observe	55	MD4 (CTRL)	Control/Observe
22	TESTM1 (CTRL)	Control/Observe	56	REDUNDANT	Observe
23	TESTM0 (IN)	Observe	57	REDUNDANT	Control/Observe
24	TESTM0 (OUT)	Control/Observe	58	REDUNDANT	Control/Observe
25	TESTM0 (CTRL)	Control/Observe	59	REDUNDANT	Observe
26	REDUNDANT	Observe	60	REDUNDANT	Control/Observe
27	REDUNDANT	Control/Observe	61	REDUNDANT	Control/Observe
28	REDUNDANT	Control/Observe	62	REDUNDANT	Observe
29	ECS (IN)	Observe	63	REDUNDANT	Control/Observe
30	ECS (OUT)	Control/Observe	64	REDUNDANT	Control/Observe
31	ECS (CTRL)	Control/Observe	65	REDUNDANT	Observe
32	REDUNDANT	Observe	66	REDUNDANT	Control/Observe
33	REDUNDANT	Control/Observe	67	REDUNDANT	Control/Observe
34	REDUNDANT	Control/Observe	68	REDUNDANT	Observe

No	Port	Type
69	REDUNDANT	Control/Observe
70	REDUNDANT	Control/Observe
71	REDUNDANT	Observe
72	REDUNDANT	Control/Observe
73	REDUNDANT	Control/Observe
74	REDUNDANT	Observe
75	REDUNDANT	Control/Observe
76	REDUNDANT	Control/Observe
77	REDUNDANT	Observe
78	REDUNDANT	Control/Observe
79	REDUNDANT	Control/Observe
80	REDUNDANT	Observe
81	REDUNDANT	Control/Observe
82	REDUNDANT	Control/Observe
83	REDUNDANT	Observe
84	REDUNDANT	Control/Observe
85	REDUNDANT	Control/Observe
86	REDUNDANT	Observe
87	REDUNDANT	Control/Observe
88	REDUNDANT	Control/Observe
89	REDUNDANT	Observe
90	REDUNDANT	Control/Observe
91	REDUNDANT	Control/Observe
92	REDUNDANT	Observe
93	REDUNDANT	Control/Observe
94	REDUNDANT	Control/Observe
95	REDUNDANT	Observe
96	REDUNDANT	Control/Observe
97	REDUNDANT	Control/Observe
98	REDUNDANT	Observe
99	REDUNDANT	Control/Observe
100	REDUNDANT	Control/Observe
101	REDUNDANT	Observe
102	REDUNDANT	Control/Observe
103	REDUNDANT	Control/Observe
104	REDUNDANT	Observe
105	REDUNDANT	Control/Observe
106	REDUNDANT	Control/Observe
107	REDUNDANT	Observe
108	REDUNDANT	Control/Observe
109	REDUNDANT	Control/Observe

No	Port	Type
110	REDUNDANT	Observe
111	REDUNDANT	Control/Observe
112	REDUNDANT	Control/Observe
113	REDUNDANT	Observe
114	REDUNDANT	Control/Observe
115	REDUNDANT	Control/Observe
116	AD0 (IN)	Observe
117	AD0 (OUT)	Control/Observe
118	AD0 (CTRL)	Control/Observe
119	AD0 (IN)	Observe
120	AD0 (OUT)	Control/Observe
121	AD1 (CTRL)	Control/Observe
122	AD2 (IN)	Observe
123	AD2 (OUT)	Control/Observe
124	AD2 (CTRL)	Control/Observe
125	AD3 (IN)	Observe
126	AD3 (OUT)	Control/Observe
127	AD3 (CTRL)	Control/Observe
128	AD4 (IN)	Observe
129	AD4 (OUT)	Control/Observe
130	AD4 (CTRL)	Control/Observe
131	AD5 (IN)	Observe
132	AD5 (OUT)	Control/Observe
133	AD5 (CTRL)	Control/Observe
134	AD6 (IN)	Observe
135	AD6 (OUT)	Control/Observe
136	AD6 (CTRL)	Control/Observe
137	AD7 (IN)	Observe
138	AD7 (OUT)	Control/Observe
139	AD7 (CTRL)	Control/Observe
140	CBE0_ (IN)	Observe
141	CBE0_ (OUT)	Control/Observe
142	CBE0_ (CTRL)	Control/Observe
143	AD8 (IN)	Observe
144	AD8 (OUT)	Control/Observe
145	AD8 (CTRL)	Control/Observe
146	AD9 (IN)	Observe
147	AD9 (OUT)	Control/Observe
148	AD9 (CTRL)	Control/Observe
149	AD10 (IN)	Observe
150	AD10 (OUT)	Control/Observe

No	Port	Type
151	AD10 (CTRL)	Control/Observe
152	AD11 (IN)	Observe
153	AD11 (OUT)	Control/Observe
154	AD11 (CTRL)	Control/Observe
155	AD12 (IN)	Observe
156	AD12 (OUT)	Control/Observe
157	AD12 (CTRL)	Control/Observe
158	AD13 (IN)	Observe
159	AD13 (OUT)	Control/Observe
160	AD13 (CTRL)	Control/Observe
161	AD14 (IN)	Observe
162	AD14 (OUT)	Control/Observe
163	AD14 (CTRL)	Control/Observe
164	AD15 (IN)	Observe
165	AD15 (OUT)	Control/Observe
166	AD15 (CTRL)	Control/Observe
167	CBE1_ (IN)	Observe
168	CBE1_ (OUT)	Control/Observe
169	CBE1_ (CTRL)	Control/Observe
170	PAR (IN)	Observe
171	PAR (OUT)	Control/Observe
172	PAR (CTRL)	Control/Observe
173	SERR_ (IN)	Observe
174	SERR_ (OUT)	Control/Observe
175	SERR_ (CTRL)	Control/Observe
176	SMBDATA (IN)	Observe
177	SMBDATA (OUT)	Control/Observe
178	SMBDATA (CTRL)	Control/Observe
179	SMBCLK (IN)	Observe
180	SMBCLK (OUT)	Control/Observe
181	SMBCLK (CTRL)	Control/Observe
182	PERR_ (IN)	Observe
183	PERR_ (OUT)	Control/Observe
184	PERR_ (CTRL)	Control/Observe
185	STOP_ (IN)	Observe
186	STOP_ (OUT)	Control/Observe
187	STOP_ (CTRL)	Control/Observe
188	DEVSEL_ (IN)	Observe
189	DEVSEL_ (OUT)	Control/Observe
190	DEVSEL_ (CTRL)	Control/Observe
191	TRDY_ (IN)	Observe

No	Port	Type
192	TRDY_ (OUT)	Control/Observe
193	TRDY_ (CTRL)	Control/Observe
194	IRDY_ (IN)	Observe
195	IRDY_ (OUT)	Control/Observe
196	IRDY_ (CTRL)	Control/Observe
197	FRAME_ (IN)	Observe
198	FRAME_ (OUT)	Control/Observe
199	FRAME_ (CTRL)	Control/Observe
200	CBE2_ (IN)	Observe
201	CBE2_ (OUT)	Control/Observe
202	CBE2_ (CTRL)	Control/Observe
203	AD16 (IN)	Observe
204	AD16 (OUT)	Control/Observe
205	AD16 (CTRL)	Control/Observe
206	AD17 (IN)	Observe
207	AD17 (OUT)	Control/Observe
208	AD17 (CTRL)	Control/Observe
209	AD18 (IN)	Observe
210	AD18 (OUT)	Control/Observe
211	AD18 (CTRL)	Control/Observe
212	AD19 (IN)	Observe
213	AD19 (OUT)	Control/Observe
214	AD19 (CTRL)	Control/Observe
215	AD20 (IN)	Observe
216	AD20 (OUT)	Control/Observe
217	AD20 (CTRL)	Control/Observe
218	AD21 (IN)	Observe
219	AD21 (OUT)	Control/Observe
220	AD21 (CTRL)	Control/Observe
221	AD22 (IN)	Observe
222	AD22 (OUT)	Control/Observe
223	AD22 (CTRL)	Control/Observe
224	AD23 (IN)	Observe
225	AD23 (OUT)	Control/Observe
226	AD23 (CTRL)	Control/Observe
227	IDSEL (IN)	Observe
228	CBE3_ (IN)	Observe
229	CBE3_ (OUT)	Control/Observe
230	CBE3_ (CTRL)	Control/Observe
231	AD24 (IN)	Observe
232	AD24 (OUT)	Control/Observe

No	Port	Type
233	AD24 (CTRL)	Control/Observe
234	AD25 (IN)	Observe
235	AD25 (OUT)	Control/Observe
236	AD25 (CTRL)	Control/Observe
237	AD26 (IN)	Observe
238	AD26 (OUT)	Control/Observe
239	AD26 (CTRL)	Control/Observe
240	AD27 (IN)	Observe
241	AD27 (OUT)	Control/Observe
242	AD27 (CTRL)	Control/Observe
243	AD28 (IN)	Observe
244	AD28 (OUT)	Control/Observe
245	AD28 (CTRL)	Control/Observe
246	AD29 (IN)	Observe
247	AD29 (OUT)	Control/Observe
248	AD29 (CTRL)	Control/Observe
249	AD30 (IN)	Observe
250	AD30 (OUT)	Control/Observe

No	Port	Type
251	AD30 (CTRL)	Control/Observe
252	AD31 (IN)	Observe
253	AD31 (OUT)	Control/Observe
254	AD31 (CTRL)	Control/Observe
255	PME_ (IN)	Observe
256	PME_ (OUT)	Control/Observe
257	PME_ (CTRL)	Control/Observe
258	REQ_ (IN)	Observe
259	REQ_ (OUT)	Control/Observe
260	REQ_ (CTRL)	Control/Observe
261	GNT_ (IN)	Observe
262	PCICLK (IN)	Observe
263	PCIRST_ (IN)	Observe
264	INTA_ (IN)	Observe
265	INTA_ (OUT)	Control/Observe
266	INTA_ (CTRL)	Control/Observe
267	AUXRSTZ (IN)	Observe

Auto-Negotiation

The VT6122 supports Auto-Negotiation, a standards-defined (IEEE 802.3-2000, Clause 28) process for determining the operating attributes of the local PHY and its link partner. Auto-Negotiation evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode.

In particular, Auto-Negotiation can determine speed, duplex, and MASTER/SLAVE modes for 1000BASE-T. Auto-Negotiation also allows the local MAC to communicate with the Link Partner MAC (via optional "Next-Pages") to set attributes that may not be defined in the standard.

The operating mode of the local PHY of the VT6122 can be set by any one of three methods:

- MII configuration control bits, or
- Auto-Negotiation.

Auto-Negotiation is used by default. Indeed, a station manager (communicating to the integrated PHY via the MAC) is optional; in the absence of a station manager, the VT6122 will auto-negotiate upon exiting reset. Autonegotiation is enabled by default during power-on reset.

If Auto-Negotiation is enabled, Auto-Negotiation will start upon any of the following conditions:

- Release of hardware reset,
- Release of software reset,
- Restart Auto-Negotiation (Register bit 0.9),
- Release of Power-Down (Register bit 0.11), or
- Entering the "link_fail" state.

Once Auto-Negotiation starts, the VT6122 will first determine if the Link Partner is Auto-Negotiation capable. If the Link Partner is Auto-Negotiation capable, the VT6122 will, by default, determine the highest-performance operating mode that is common between the local PHY and the Link Partner's PHY. If the Link Partner is not Auto-Negotiation capable, the VT6122 will use Parallel-Detect to set the operating mode.

Auto MDI / MDI-X Function

For trouble-free configuration and management of Ethernet links, the VT6122 includes robust Automatic Crossover Detection functionality for all three speeds (10BASE-T, 100BASE-TX, and 1000BASE-T) – fully compliant with the IEEE standard. In addition, the VT6122 detects and corrects polarity errors on *all* MDI pairs, which is not required by the standard. Both the Automatic MDI/MDI-X and Polarity Correction functions are enabled by default.[17] However, complete user control of these two features is contained in MII Registers 18.5 (Automatic MDI/MDI-X Correction) and 18.4 (Automatic Polarity Correction). Status bits for each of these functions are indicated in MII Registers 26.6 and 26.5. For all three speeds of operation, any of the following MDI pair (A, B, C, D) connection combinations may be supplied to the device, with complete automatic detection and correction by the VT6122.

The VT6122's Automatic MDI/MDI-X algorithm will successfully detect, correct, and operate with any of the MDI wiring pair combinations listed in the following table.

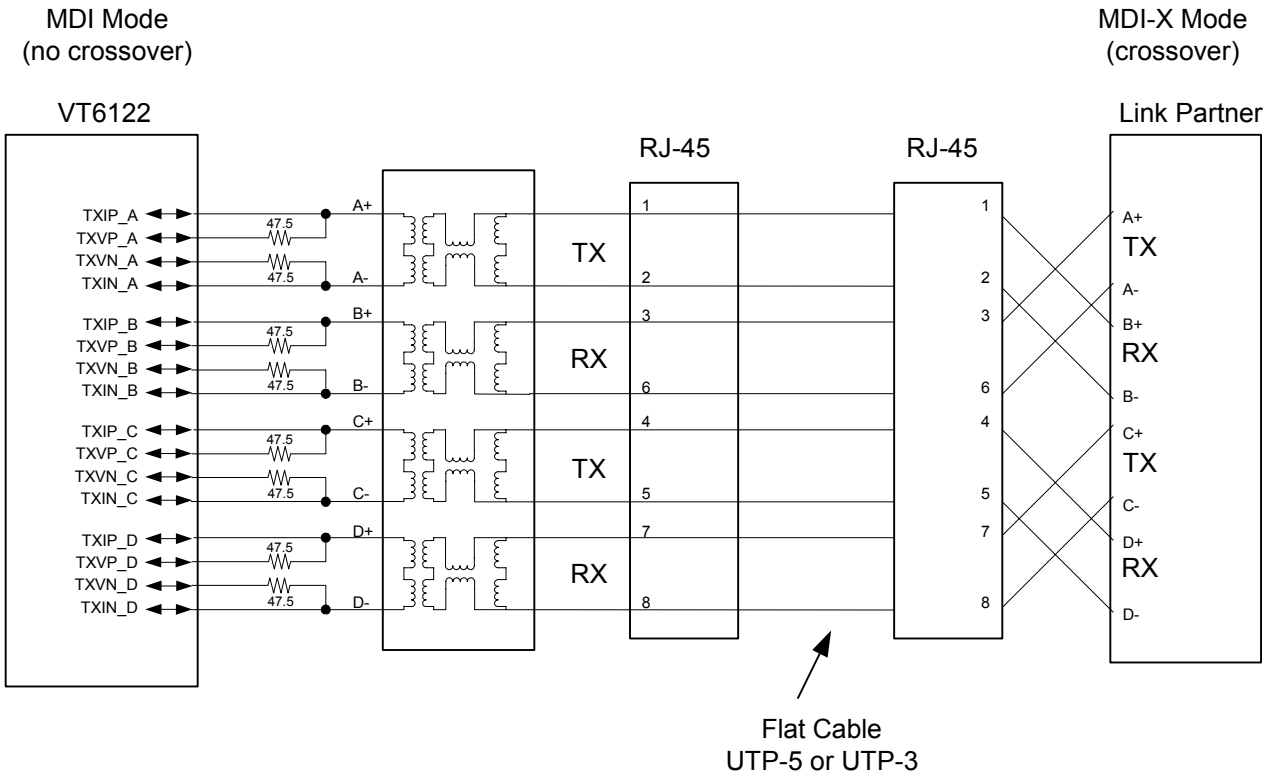
Table 21. Accepted MDI Pair Connection Combinations

	RJ-45 Connections				Comments
	1,2	3,6	4,5	7,8	
MDI Pair Connection Combinations Accepted by VT6122	A	B	C	D	Normal MDI mode Normal DTE/NIC mode No crossovers
	B	A	C	D	MDI-X mode Normal for switches & repeaters Crossover on A and B pairs only
	A	B	D	C	Normal MDI mode Normal for DTEs (NICs) No crossovers Pair swap on C and D pairs
	B	A	D	C	Normal MDI-X mode Normal switch/repeater mode Crossovers assumed Crossover on A and B pairs Pair swap on C and D pairs

The diagram below depicts the last combination in the table above, showing the VT6122 operating with a link partner with crossovers on all four MDI pairs.

[17] Consistent with 10/100/1000BASE-T PHYs on the market today, Auto MDI/MDI-X functionality is automatically disabled when Auto-Negotiation is disabled.

Figure 10. MDI / MDI-X Crossover Example



ActiPHY™ Power Management

In addition to the IEEE-specified (i.e., Register bit 0.11 = 1) and "sleep" power management modes, the VT6122's ActiPHY™ power management mode enables support for power-sensitive applications such as laptop computers with Wake-on-LAN capability by utilizing a signal-detect function[18].

When the Station Manager detects that the PHY has not established a link for an arbitrary amount of time (determined by the Station Manager), it can put the PHY in a low-power energy-detect state by setting the ActiPHY™ Enable bit (MII Register bit 23.5). In response, the PHY powers down all unused blocks, stops auto-negotiating, and enables the logic block that generates an interrupt when valid energy levels are detected on the media interface. The Station Manager also sets the Link State-Change/ActiPHY™ interrupt mask bit (25.13) so that the PHY can generate an interrupt in response to a signal-detect event. With bits 23.5, 25.15, and 25.13 all set to "1", the Interrupt Status Register (MII Register 26) must be read in order to automatically clear any pending interrupts. The PHY will only respond to the presence of valid network energy levels (listed in MII Register 22.11:10) when in this mode; it does not attempt to establish a link.

When the PHY does detect energy on the media interface, it sends an interrupt to the Station Manager if bits 25.15 and 25.13 are set to "1". In response, the Station Manager must clear bit 23.5, which automatically brings the VT6122 out of the ActiPHY™ low-power mode and allows it to establish a link.

[18]See Wake-on-LAN Design Considerations Application note for further details.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 22. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_S	Storage Temperature	-55	—	125	°C
T_C	Case temperature, directly above chip center	0	—	70	°C
V_{CC}	3.3V I/O Supply Voltage	—	3.3	—	V
V_{DD}	1.5V Core Voltage	—	1.5	—	V
V_{DDA}	1.5V Analog Part Voltage	—	1.5	—	V
V_{DDRAM}	1.5V Internal SRAM Voltage	—	1.5	—	V
—	ESD HBM Rating	—	—	±2000	V

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Specifications

Tc = 0-70° C, V_{DD} = V_{DDRAM} = V_{DDA} = 1.5V±5%, V_{CC} = 3.3V±5%, GND = 0V

Table 23. DC Specifications

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	–0.5	0.8	Volt	
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{OL}	Output Low Voltage	—	0.45	Volt	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	—	Volt	I_{OH} = –1.0 mA
I_{IL}	Input Leakage Current	—	±10	uA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate Leakage Current	—	±20	uA	$0.45 < V_{OUT} < V_{CC}$

Note: **These parameters are not guaranteed by production testing, All electrical specifications are based on IEEE 802.3 requirements and internal design considerations.**

Table 24. Current Consumption

	1000BT			100BT			10BT		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
$I_{3.3V}$	TBD	350	TBD	TBD	133	TBD	TBD	116	TBD
$I_{1.5V}$	TBD	400	TBD	TBD	140	TBD	TBD	50	TBD

Unit: mA

Timing Specifications

Auto-Negotiation Fast Link Pulse (FLP) Timing

The following specifications represent both transmit and receive timings. They are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 1.5V, 5%. See MII Register 23 for more information.

Table 25. Auto-Negotiation FLP AC Timing Specification

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{CLK-Period}$	14	121	139	µs	Clock pulse to clock pulse period.
$T_{CLK/DATA}$		100		ns	Clock/Data pulse width.
$T_{CLK/DATA-Period}$		62.5		µs	Clock pulse to data pulse period (Data = 1).
$T_{BURST-Period}$	8		24	ms	FLP burst to FLP burst period.
T_{BURST}		11		ms	FLP burst width.
n_{BURST}	17		33	#	Number of pulses in an FLP burst.

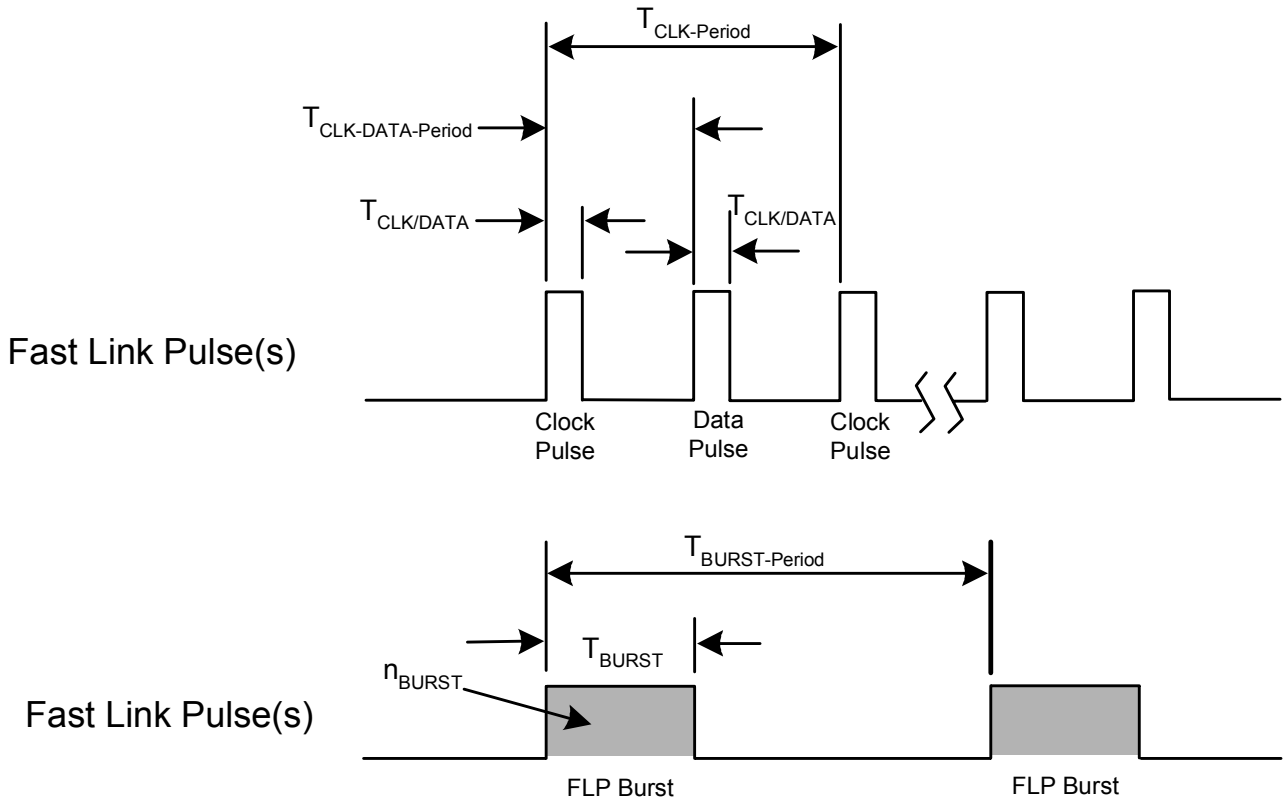


Figure 11. Auto-Negotiation FLP AC Timing

JTAG Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, 5%. See MII Register 23 for more information.

Table 26. JTAG Interface AC Timing Specification

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{TCK\text{-}Period}$	100			ns	TCK period.
$T_{TCK\text{-}High}$	45			ns	TCK minimum pulse width high.
$T_{TCK\text{-}Low}$	45			ns	TCK minimum pulse width low.
$T_{TDI/TMS\text{-}Setup}$	10			ns	(TMS or TDI) to TCK setup time.
$T_{TDI/TMS\text{-}Hold}$	10			ns	(TMS or TDI) to TCK hold time.
$T_{TDO\text{-}Delay}$	0		15	ns	TDO delay from TCK.

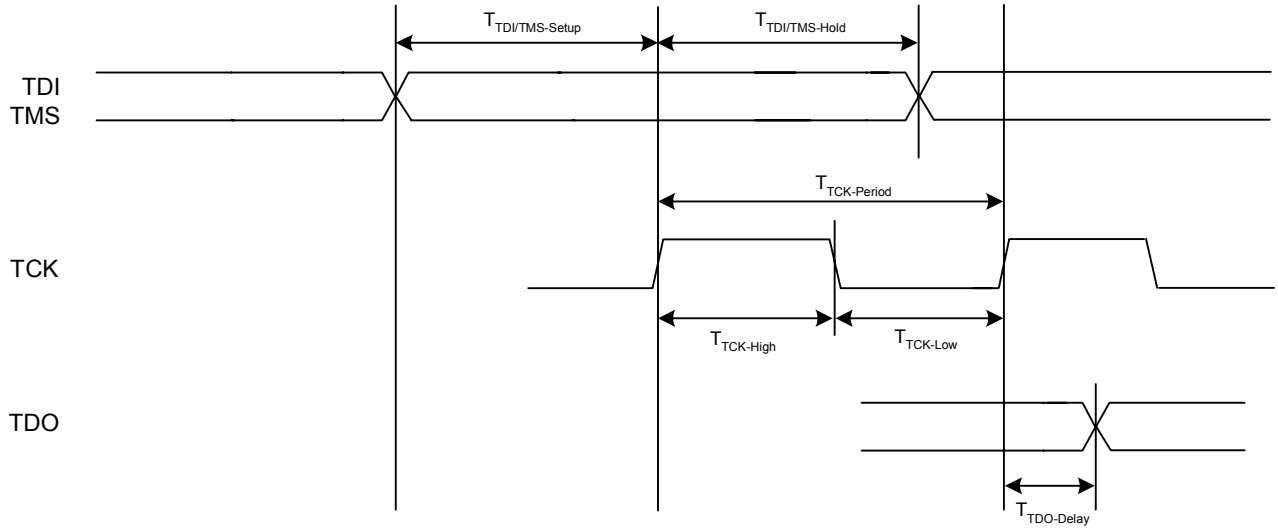


Figure 12. JTAG Interface AC Timing

X1/REFCLK Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, 5%. See MII Register 23 for more information.

Table 27. REFCLK AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
$T_{REFCLK25}$		40		Ns	Reference clock period, PLLMODE = 0 (25MHz reference).
$F_{STABILITY}$	-100		+100	ppm	Reference clock frequency stability (0 C to 70 C).
T_{DUTY}	40		60	%	REFCLK duty cycle in both 25MHz and 125MHz modes.
$J_{REFCLK25,}$			100	ps	Total jitter of 25MHz clock (peak-to-peak).
$t_{R/F\ (REFCLK25)}$			4	ns	Reference clock rise time, 25MHz mode (20% to 80%).

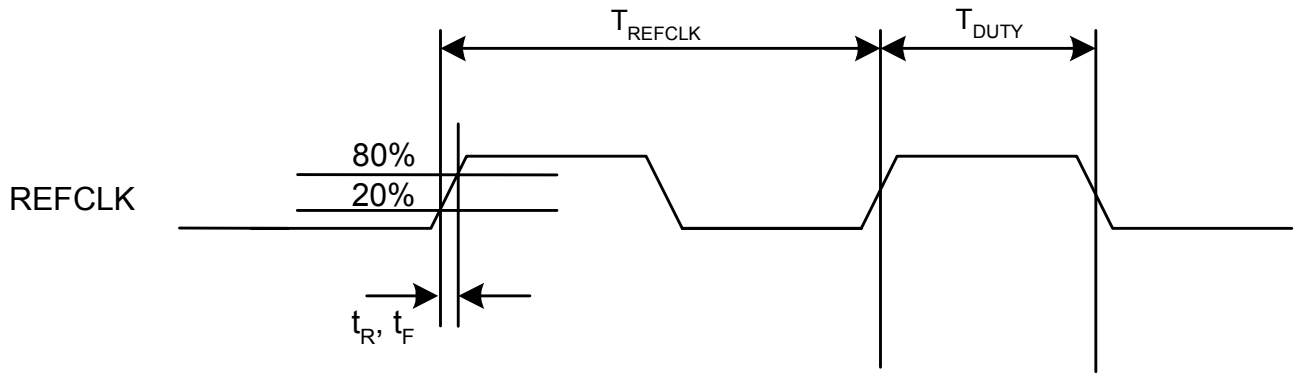


Figure 13. X1/REFCLK AC Timing

Regulator Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, 5%. See MII Register 23 for more information.

Table 28. Regulator AC Timing Specifications

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
T_{REG}		1		ms	Regulator start-up time.

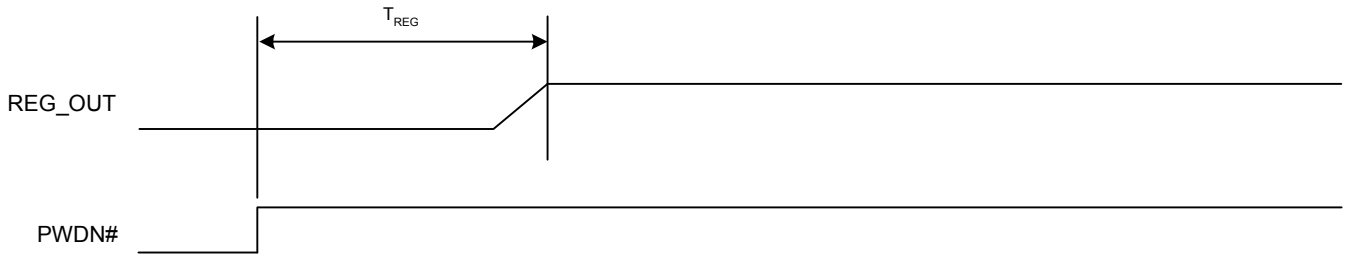


Figure 14. Regulator AC Timing

Oscillator Timing

The following specifications are valid only when the I/O power supply (VDDIO) is at either 3.0-3.6V, or 2.5V, 5%. See MII Register 23 for more information.

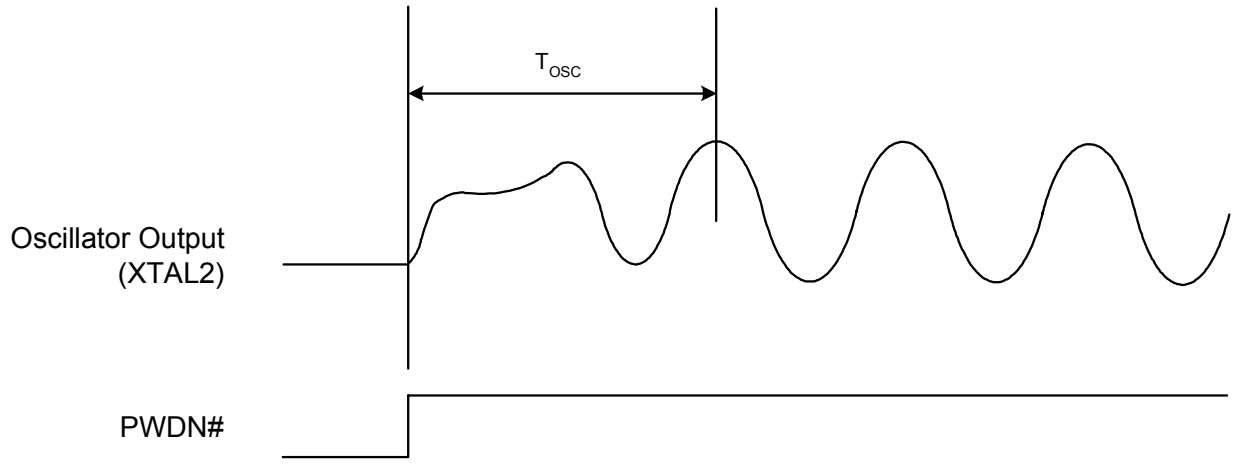


Figure 15. Oscillator AC Timing

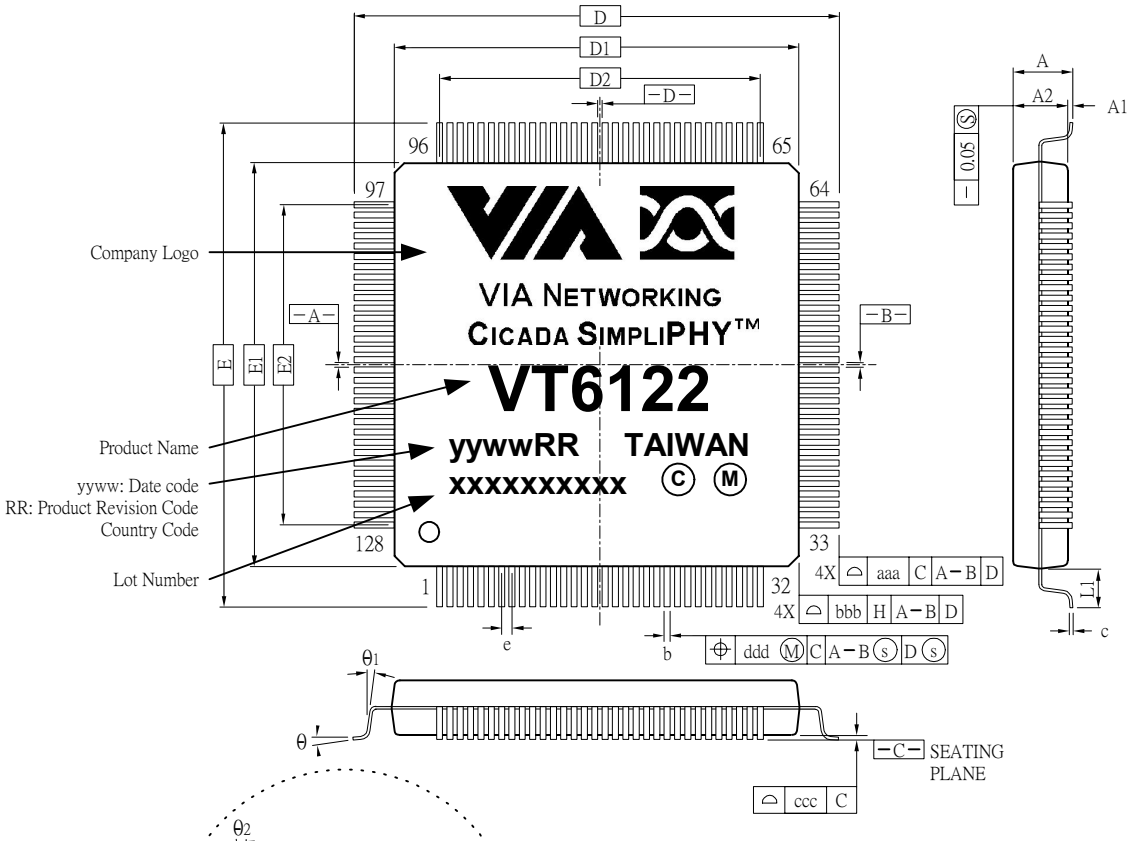
Magnetics Specifications

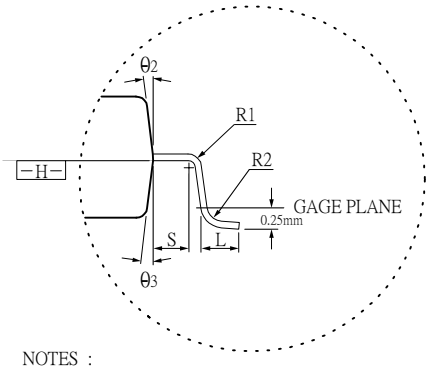
Two of the recommended transformer modules for the VT6122's twisted pair interface are:

1. Pulse Model #H5007
2. Pulse Model #H5008

Symbol	Min	Typ	Max	Unit	Parameter Description & Conditions
N		1:1		N/A	Transformer turns ratio.
-			1.0	dB	Insertion loss (60MHz to 100MHz).
-	-16			dB	Return loss, @ 85, 100, 115Ω (1MHz to 40MHz).
-	$10 - 20\log_{10}$ (f/80MHz)			dB	Return loss, @ 85, 110, 115Ω (40MHz to 100MHz).
-			1.5	kV	Isolation.
L_{PRI}	350			µH	Primary inductance.

MECHANICAL SPECIFICATIONS





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	12.40 BASIC			0.488 BASIC		
E2	12.40 BASIC			0.488 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BASIC			0.016 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

Figure 16. 128-Pin EP-LQFP Package

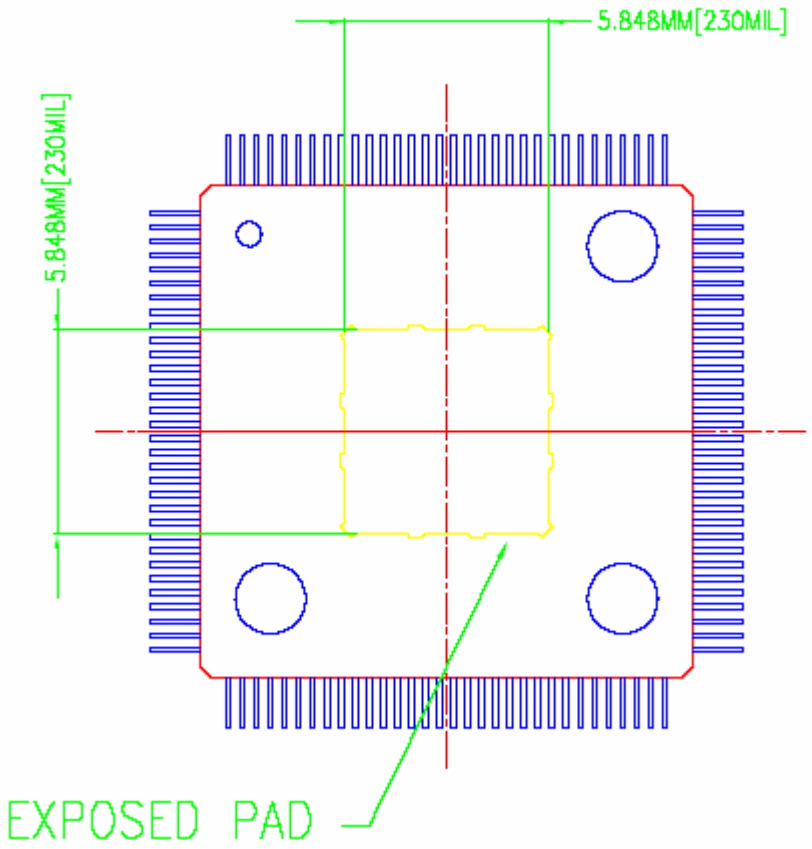


Figure 17. Bottom view of 128-Pin EP-LQFP