MX98713A

FAST ETHERNET MAC CONTROLLER

1. FEATURES

* Integrates fast Ethernet MAC, NWAY, 100 Base-TX PCS and 10 Base-T tranceive in a single chip.
* Fully comply to IEEE 802.3u specification
* MII/SYM interface to support STP and CAT5 UTP cable.
* Support full duplex operation in both 100 Base-TX and 10 Base-T mode.
* Magic Packet TM mode to support remote wake up and remote power on.
* On chip 100 Base-TX PCS and 10 Base-T transceiver with filter.
* 100/10 Base-T NWAY auto negotiation function.
* Large on chip FIFOs for both transmit and receive operations without external local memory
* Fully comply to PCI spec. 2.1 with bus clock ranges from 16 MHz to 33 MHz.
* PCI Bus master architecture with linked host buffers delivers excellent performance.
* 32-bit bus master DMA channel provides ultra low CPU utilization.
* Support up to 256K bytes boot ROM and FLASH interface
* Two levels of loopback diagnositic capability
* Support a variety of flexible address filtering modes with 16 CAM address and 512 bits hash.
* MicroWire interface to EEPROM for customer's IDs and configuration data.
* 160 PQFP package with CMOS technology, pin-to-pin compatible to MX98713

(Magic Packet Technology is a trademark of Advanced Micro Device Corp.)

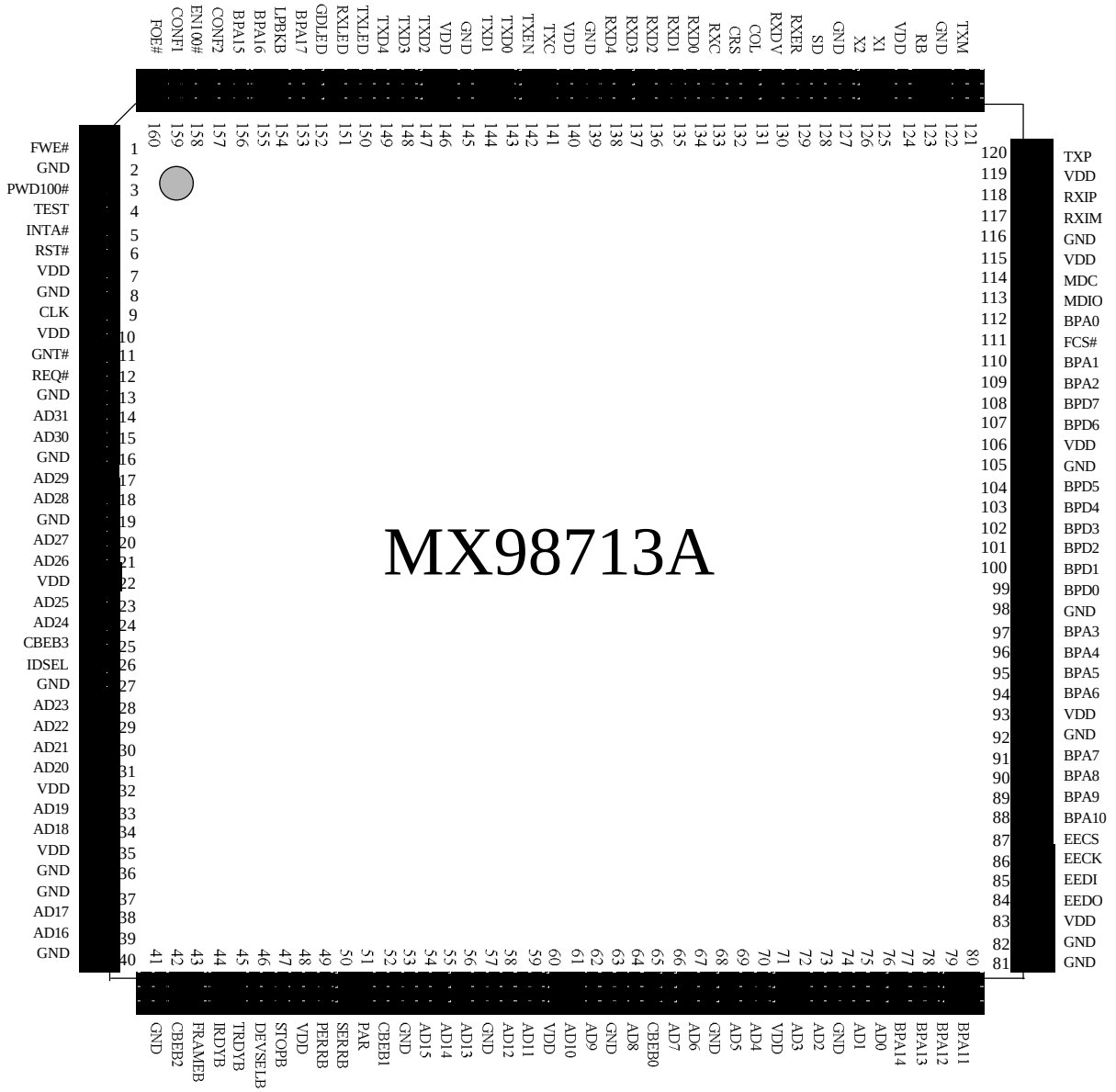
2. GENERAL DESCRIPTION

The MX98713A Fast Ethernet controller is designed to interface directly with PCI bus and 100/10 Base-T Fast Ethernet with MII/SYM interface and a 10 Base-T transceiver to support NWAY autonegotiation with any 100 Base-TX PHY/PMD chips. Together with MX98702 (100 Base-TX PMD) and MX98704 (100 Base-TX PHY), or with a MX98705 (100 Base-TX PHY/PMD combo) chip creates a total solution for Fast Ethernet adaptor application.

High speed PCI bus master interface with large on chip FIFOs, the MX98713A provides a cost effective solution that delivers excellent performance. Nway function enables user to plug in cable and link up the network automatically. Magic Packet based advanced power management not only save electric energy but also provides network maintenance efficiency through the application of Remote-Wake-Up and

Remote-Power-On. This feature is most valuable for high-end green PCs and intelligent LAN environment. Full duplex and half duplex are both supported. A packet buffer is located in the host memory that is used by MX98713A`s device driver for all incoming and outgoing packets. This buffer area is shared by both transmit process and receive process. During reception, the MX98713A stores packets in the receive buffer area, then indicates receive status and control information in the descriptor area. This packet buffer is also used by transmit process which can transmit multiple packets from a single transmit command. Back-to-back packets at full line speed in 100 Base-TX mode is effortless with MX98713A.

3. PIN CONFIGURATIONS



4. PIN DESCRIPTION (160 PIN PQFP)

(T/S : tri-state, S/T/S : sustended tri-state, I : input, O : output, O/D : open drain)

Pin Name	Type	160 Pin Function and Driver
AD[31:0]	**I/O**	**PCI address/data bus**: shared PCI address/data bus lines. Little or big endian byte ordering are supported.
CBE[3:0]	**I/O**	**PCI command and byte enable bus**: shared PCI command byte enable bus, during the address phase of the transaction, these four bits provide the bus command. During the data phase, these four bits provide the byte enable.
FRAMEB	**I/O**	**PCI FRAME# signal**: shared PCI cycle start signal, asserted to indicate the beginning of a bus transaction. While FRAMEB is asserted, data transfers continue.
TRDYB	**I/O**	**PCI Target ready**: issued by the target agent, a data phase is completed on the rising edge of PCICLK when both IRDYB and TRDYB are asserted.
IRDYB	**I/O**	**PCI Master ready**: indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of PCICLK when both IRDYB and TRDYB are asserted.
DEVSELB	**I/O**	**PCI slave device select**: asserted by the target of the current bus access. When 98713A is the initiator of current bus access, the target must assert DEVSELB within 5 bus cycles, otherwise cycle is aborted.
IDSEL	**I**	**PCI initialization device select**: target specific device select signal for configuration cycles issued by host
PCICLK	**I**	**PCI bus clock input**: PCI bus clock targeted at 33MHZ
PRSTB	**I**	**PCI bus reset**: host system hardware reset
INTAB	**O/D**	**PCI bus interrupt request signal**: wired to INTAB lines

Pin Name	Type	160 Pin Function and Driver
SERRB	**I/O**	**PCI bus system error signal**: If an address parity error is detected and CFCS bit 8 is enabled, SERR# and CFCS's bit 30 will be asserted. 6mA tristate driver
PERRB	**I/O**	**PCI bus data error signal**: As a bus master, when a data parity error is detected and CFCS bit 8 is enabled, CFCS bit 24 and CSR5 bit 13 will be asserted. As a bus target, a data parity error will cause PERR# to be asserted.
PAR	**I/O**	**PCI bus parity bit**: shared PCI bus even parity bit for 32 bits AD bus and CBE bus.
STOPB	**I/O**	**PCI Target requested transfer stop signal**: as bus master, assertion of STOP# cause PMAC either to retry, disconnect, or abort.
REQB	**O**	**PCI bus request signal**: to initiate a bus master cycle request
GNTB	**I**	**PCI bus grant acknowledge signal**: asserts to indicate to PMAC that access to the bus is granted
TXLED	**O**	**TX activity indicator** : diecrtly sink external LED circuit with a serial resistor of 270-330 Ohm.
RXLED	**O**	**RX activity indicator**: directly sink external LED cuircuit with a serial resistor of 270-330 ohm.
GDLED	**O**	**Good Link/Signal detect indicator**: diecrtly sink external LED circuit with a serial resistor, indicating good link in 10Base-T setup or Signal Detect Good in 100Base-TX setup.
BPA17	**O**	**Boot PROM address bit 17**:driven by MX98713A, together with BPA[17 :0] to access external boot PROM up to 256KB
LPBKB	**O**	**PHY device external loopback control**: driven by MX98713A to force PHY device to do loopback.
BPA16	O	**Boot PROM address bit 16**: driven by MX98713A, together with BPA[17 :0] to access external boot PROM up to 256KB
BPA15	**O**	**Boot PROM address bit 15**: driven by MX98713A, together with BPA[17 :0] to access external boot PROM up to 256KB.

Pin Name	Type	160 Pin Function and Driver
BPA[14:0]	**O**	**Boot RPOM address lines**: driven by MX98713A, together with BPA15 can access external bootPROM up to 64KB.
MDC	**O**	**MII management interface clock**: sourced by MX98713A
MDIO	**I/O**	**MII management interface IO data bit**:
EECS	**O**	**Net ID ROM chip select**:
EECK	**O**	**Net ID ROM interface clock output**:
EEDI	**O**	**Net ID ROM input data bit**:
EEDO	**I**	**Net ID ROM output data bit**:
SD	**I**	**Signal detect indication**: supplied by external PMD device.
COL	**I**	**Collision detect of MII/SYM interface**: sourced by external physical layer protocol (PHY) device**.**
CRS	**I**	**Carrier sense of MII/SYM interface**: sourced by external physical layer protocol (PHY) device**.**
RXDV	**I**	**Receive data valid signal of MII/SYM interface**: asserted by external PHY when receive data is presented on MII_RXD lines**.**
RXER	**I**	**Receive error signal of MII/SYM interface**: synchronous to MII_RXC and asserted by external PHY when a data decoding error occures

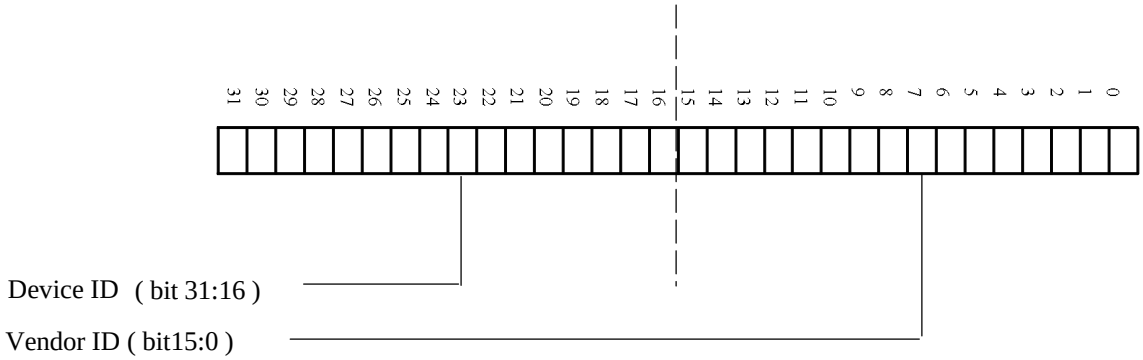
Pin Name	Type	160 Pin Function and Driver
TXP	**O**	**Twisted pair transmit differential output**: Together with TXM provides 10 Base-T transmit differential output
TXM	**O**	**Twisted pair transmit differential output**: Together with TXP provides 10 Base-T transmit differential output
RB	**I**	**Bias control**: A external resistor (12k ohms, 5% accuracy) connects this pin to ground for operating bias control
X1	**I**	**Crystal or external oscillator input**: frequencies of 20Mhz, used by 10 Base-T interface.
X2	**O**	**Crystal feedback output**: Used in crystal connections only. Should be left completely unconnected when using an oscillator module.
EN100B	**O**	**External 100 TX enable**: set to disable external 100Base-TX transceiver, reset to enable external 100Base-TX transceiver, it can be used to drive external port LED.
PWD100B	**O**	**Power Down external 100 Base-TX PHY/PMD** : Whenever Magic Packet mode or sleep mode is set, this pin goes low until a recovery event occur when this pin will be asserted high. It can be used to wake-up the host system.
CONF2	**I**	**Configuration input bit 2**: Should be unconnected for normal operation
CONF1	**I**	**Configuration input bit 1**: Should be unconnected for normal operation
FWEB	**O**	**Flash Write Enable**: Used in the boot ROM interface.
SNSEL	**I**	**Serial mode select**: Together with SPDSEL pin defines 4 operation modes. See SPDSEL pin description for details.
BPSCR	**I**	**Bypass Scrambler mode**: When set to low enables scrambler function and MII/SYM port transmits and receives scrambler symbols. When reset to by-pass scrambler/descrambler function. .
FOEB	**O**	**Flash Output Enable**: Used in the boot ROM/Flash interface.
TEST	**I**	**TEST pin**: Set high for test mode, normally grounded.

Pin Name	Type	160 Pin Function and Driver
RXC	**I**	**Receive clock of MII/SYM interface**: supports either 25MHz or 2.5 MHz clock. Sourced by external PHY.
RXD[3:0]	**I**	**Parallel Receive data lines**: driven by external PHY and is synchronous to RXC clock. In MII mode, these are received 4 data lines. In PCS mode, combined with SYM_RXD4 forms 5 parallel data lines in symbol form.
RXD4	**I**	**Received data line in SYM mode**: MSB bit of received symbol data
TXC	**I**	**Transmit clock of MII/SYM interface**: supports either 25MHz or 2.5 MHz clock. Sourced by external PHY.
TXD[3:0]	**O**	**Parallel Transmit data lines**: drievn by PMAC synchronously to TXC clock. Data is latched by external PHY at the rising edge of TXC.
TXD4	**O**	**Transmit data line in PCS mode**: together with MII/SYM_TXD[3:0] provide five parallel lines of data in symbol form in SYM mode.
TXEN	**O**	**Transmit enable signal of MII/SYM interface**:
BPD[7:0]	**I**	**Boot ROM data lines**: byte wide data bus
RXIP	**I**	**Twisted pair receive differential input**: together with RXIM provides 10 Base-T differential receive input.
RXIM	**I**	**Twisted pair receive differential input**: together with RXIP provides 10 Base-T receive differential input.

5. PROGRAMMING INTERFACE

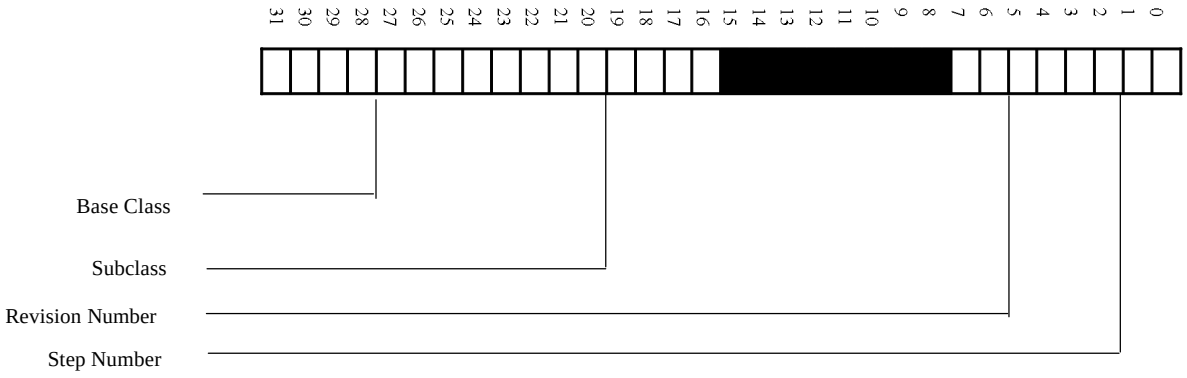
5.1 PCI CONFIGURATION REGISTERS:

5.1.1 PCI ID REGISTER (PFID) (Offset 03h-00h)



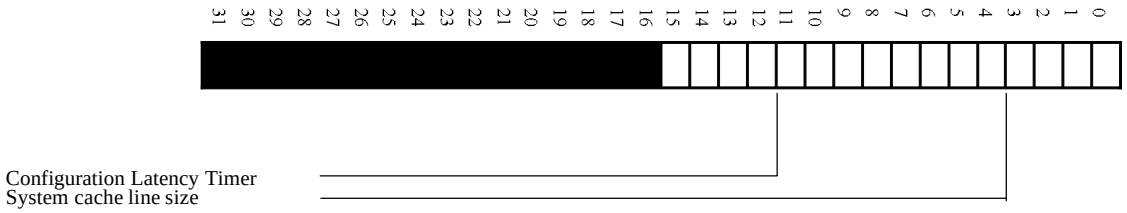
This register can be loaded from external serial EEPROM or use a MXIC preset value of "10D9" and "0531" for vendor ID and device ID respectively. Word location 3Eh and 3Dh in serial EEPROM are used to configure customer's vendor ID and device ID respectively. If location 3Eh contains "FFFF" value then MXIC's vendor ID and device ID will be set in this register, otherwise both 3Eh and 3Dh will be loaded into this register from serial EEPROM.

5.1.2 PCI REVISION REGISTER (PFRV) (Offset 0Bh-08h)



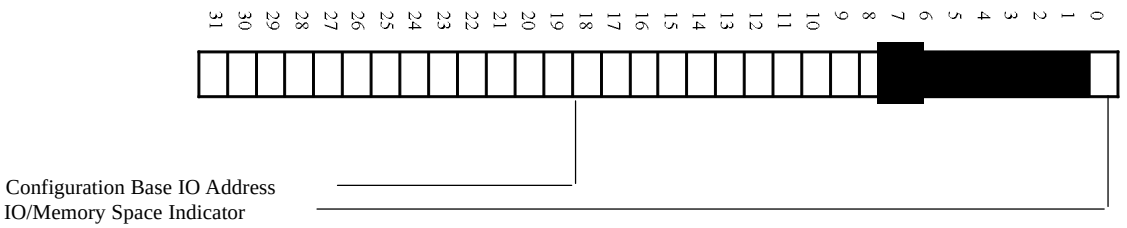
bit 3 - 0 : Step Number, range from 0 to Fh.
bit 7 - 4 : Revision Number, fixed to 1h for MX98713A
bit 15 - 8 : not used
bit 23 - 16 : Subclass, fixed to 0h.
bit 31 - 24 : Base Class, fixed to 3h.

5.1.3 PCI LATENCY TIMER REGISTER (PFLT) (Offset 0Fh-0Ch)



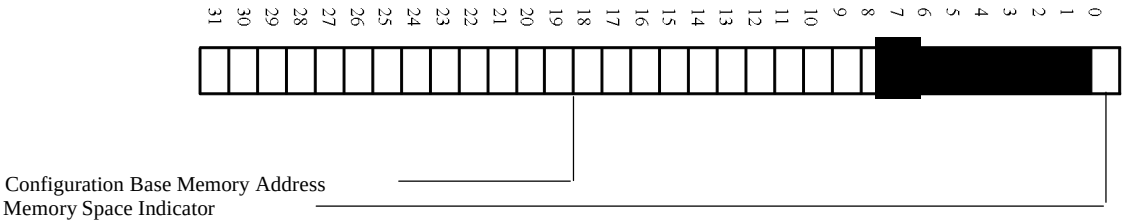
bit 0 - bit 7 : System cache line size in units of 32 bit word, device driver should use this value to rogramCSR0<15:14>.
bit 8 - bit 15 : Configuration Latency Timer, when MX98713A assert FRAME#, it enables its latency timer to count. If MX98713A deasserts FRAME# prior to timer expiration, then timer is ignored. Otherwise, after timer expires, MX98713A initiates trans action termination as soon as its GNT# is deasserted.

5.1.4 PCI BASE IO ADDRESS REGISTER (PBIO) (Offset 13h-10h)



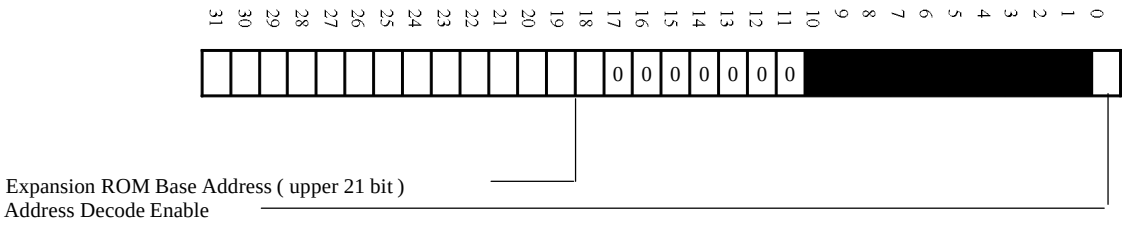
bit 0 : IO/Memory Space Indicator, fixed to 1 in this field will map into the IO space. This is a read only field.
bit 7 - 1 : not used, all 0 when read
bit 31 - 8 : Defines the address assignment mapping of MX98713A CSR registers.

5.1.5 PCI BASE MEMORY ADDRESS REGISTER (PBMA) (Offset 17h-14h)



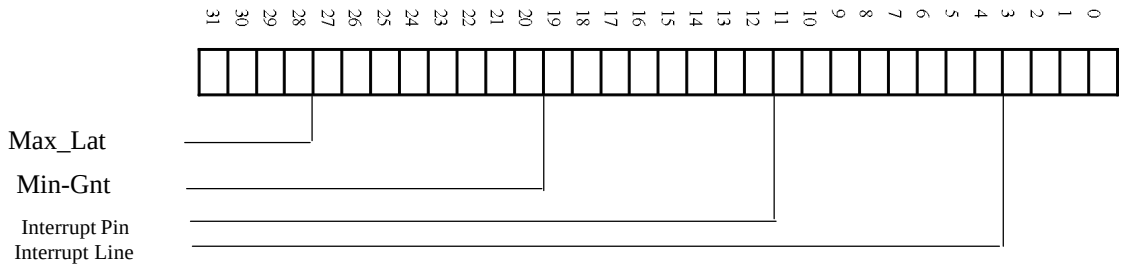
bit 0 : Memory Space Indicator, fixed to 0 in this field will map into the memory space. This is a read only field.
bit 6 - 1 : not used, all 0 when read
bit 31 - 7 : Defines the address assignment mapping of MX98713A CSR registers.

5.1.6 PCI BASE EXPANSION ROM ADDRESS REGISTER (PBER) (Offset 33h-30h)



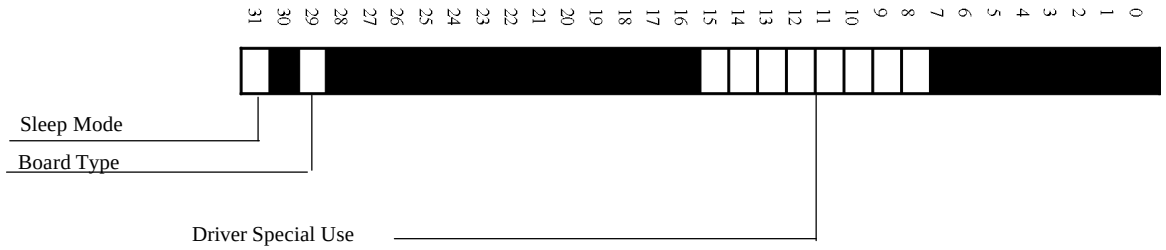
bit 0 : Address Decode Enable, decoding will be enabled if only both enable bit in PFCS<1> and this expansion ROM register are 1.
bit 10 - 1 : not used
bit 31 - 11 : Defines the upper 21 bits of expansion ROM base address.

5.1.7 INTERRUPT REGISTER (PFIT) (Offset 3Fh-3Ch)



bit 7 - 0 : Interrupt Pin, fixed to 01h which use INTA#.
bit 15 - 8 : Interrupt Line, system BIOS will writes the routing information into this field, driver can use this information to determine priority and interrupt vector.
bit 31 - 24 : Max_Lat which is a maximum period for a access to PCI bus.
bit 23 - 16 : Min_Gnt which is the maximum period that MX9713A needs to finish a brust PCI cycle.

5.1.8 PCI DRIVER AREA REGISTER (PFDA) (43h-40h)



bit 31 : Sleep Mode, set to sleep mode which allows access to PCI configuration space, a hardware reset or reset to this bit can exit from sleep mode. Magic packet can be received under sleep mode if CSR16<22> (Magic Packet Enable) is set.
bit 30 : not used
bit 29 : board type
bit 15 - 8 : driver is free to read and write this field for any purpose.
bit 7 - 0 : not used.

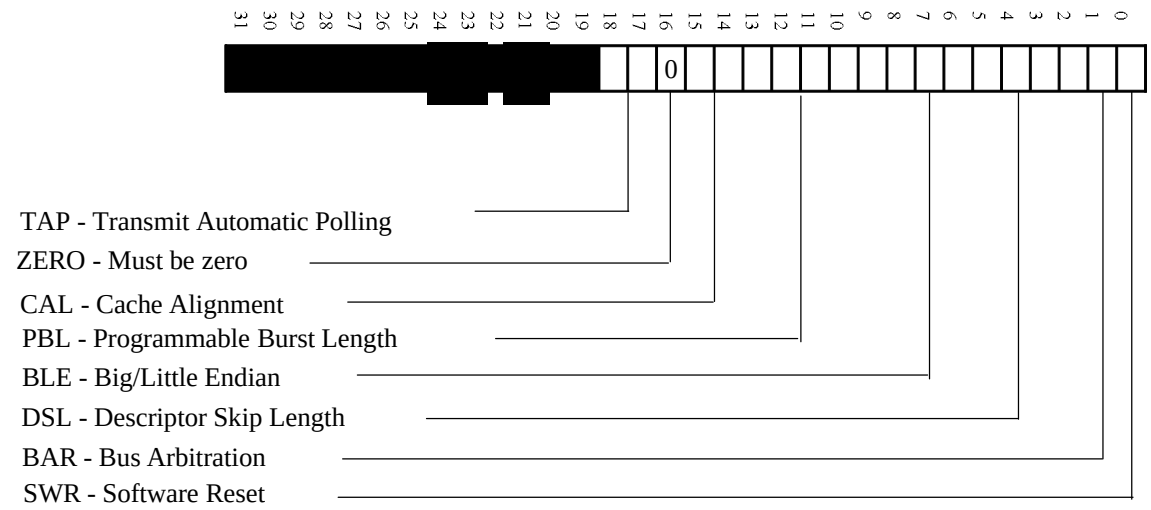
5.2 HOST INTERFACE REGISTERS

MX98713A CSRs are located in the host I/O or memory address space. The CSRs are double word aligned and 32 bits long. Definitions and address for all CSRs are as follows :

CSR Mapping

Register	Meaning	Offset from CSR Base Address (PBIO and PBMA)
CSR0	Bus mode	00h
CSR1	Transmit poll demand	08h
CSR2	Receive poll demand	10h
CSR3	Receive list demand	18h
CSR4	transmit list base address	20h
CSR5	Interrupt status	28h
CSR6	Operation mode	30h
CSR7	Interrupt enable	38h
CSR8	Missed frame counter	40h
CSR9	Serial ROM and MII management	48h
CSR10	reserved	50h
CSR11	General Purpose timer	58h
CSR12	10 Base-T status port	60h
CSR13	SIA Reset Register	68h
CSR14	10 Base-T control port	70h
CSR15	Watchdog timer	78h
CSR16	Magic Packet Register	80h

5.2.1 BUS MODE REGISTER (CSR0)

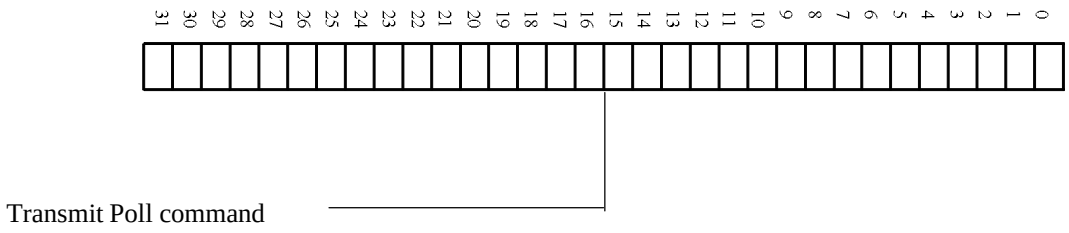


Field	Name	Description
0	SWR	Software Reset, when set, MX98713A resets all internal hardware with the exception of the configuration area and port selection.
1	BAR	Internal bus arbitration scheme between receive and transmit processes. The receive channel usually has higher priority over transmit channel when receive FIFO is partially full to a threshold. This threshold can be selected by programming this bit. Set for lower threshold, reset for normal threshold.
6:2	DSL	Descriptor Skip Length, specifies the number of longwords to skip between two descriptors.
7	BLE	Big/Little Endian, set for big endian byte ordering mode, reset for little endian byte ordering mode, this option only applies to data buffers
13:8	PBL	Programmable Burst Length, specifies the maximum number of longwords tobe transferred in one DMA transaction. default is 0, possible values can be 1,2,4,8,16, and 32.
15:14	CAL	Cache Alignment, programmable address boundaries of data burst stop, MX98713A can handle non-cache-aligned fragement as well as cache-aligned fragment efficiently.
18:17	TAP	Transmit Auto-Polling time interval, defines the time interval for MX98713A to performs transmit poll command automatically at transmit suspended state.

TABLE 5.2.0 TRANSMIT AUTO POLLING BITS

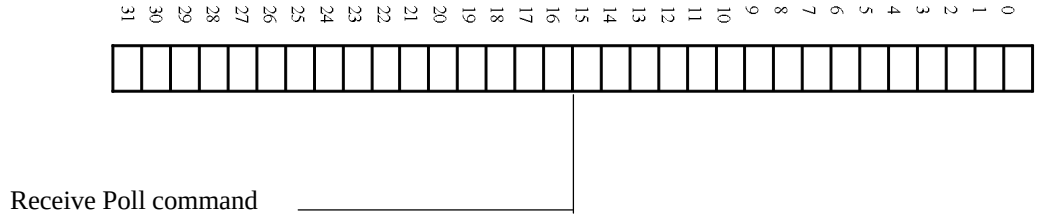
CSR<18:17>	Time Interval
00	No transmit auto-polling, a write to CSR1 is required to poll
01	auto-poll every 200 us
10	auto-poll every 800 us
11	auto-poll every 1.6 ms

5.2.2 TRANSMIT POLL COMMAND (CSR1)



Field	Name	Description
31:0	TPC	Write only, when written with any value, MX98713A read transmit descriptor list in host memory pointed by CSR4 and processes the list.

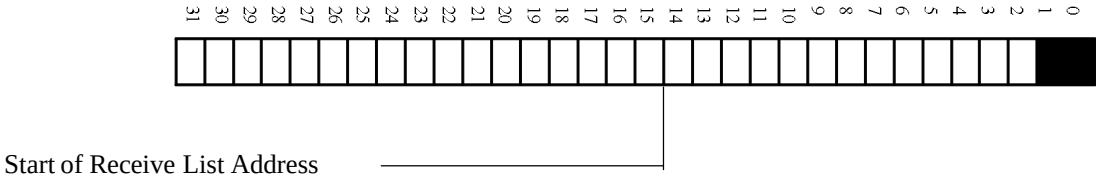
5.2.3 RECEIVE POLL COMMAND (CSR2)



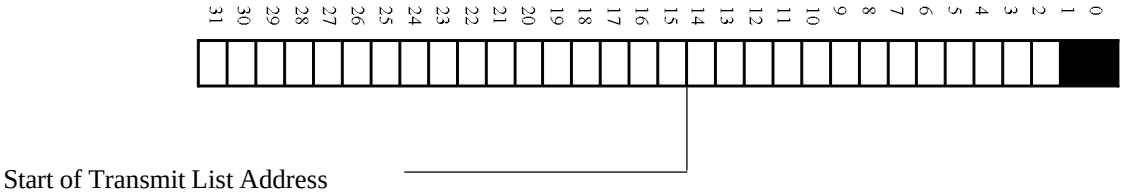
Field	Name	Description
31:0	RPC	Write only, when written with any value, MX98713A read receive descriptor list in host memory pointed by CSR4 and processes the list.

5.2.4 DESCRIPTOR LIST ADDRESS (CSR3, CSR4)

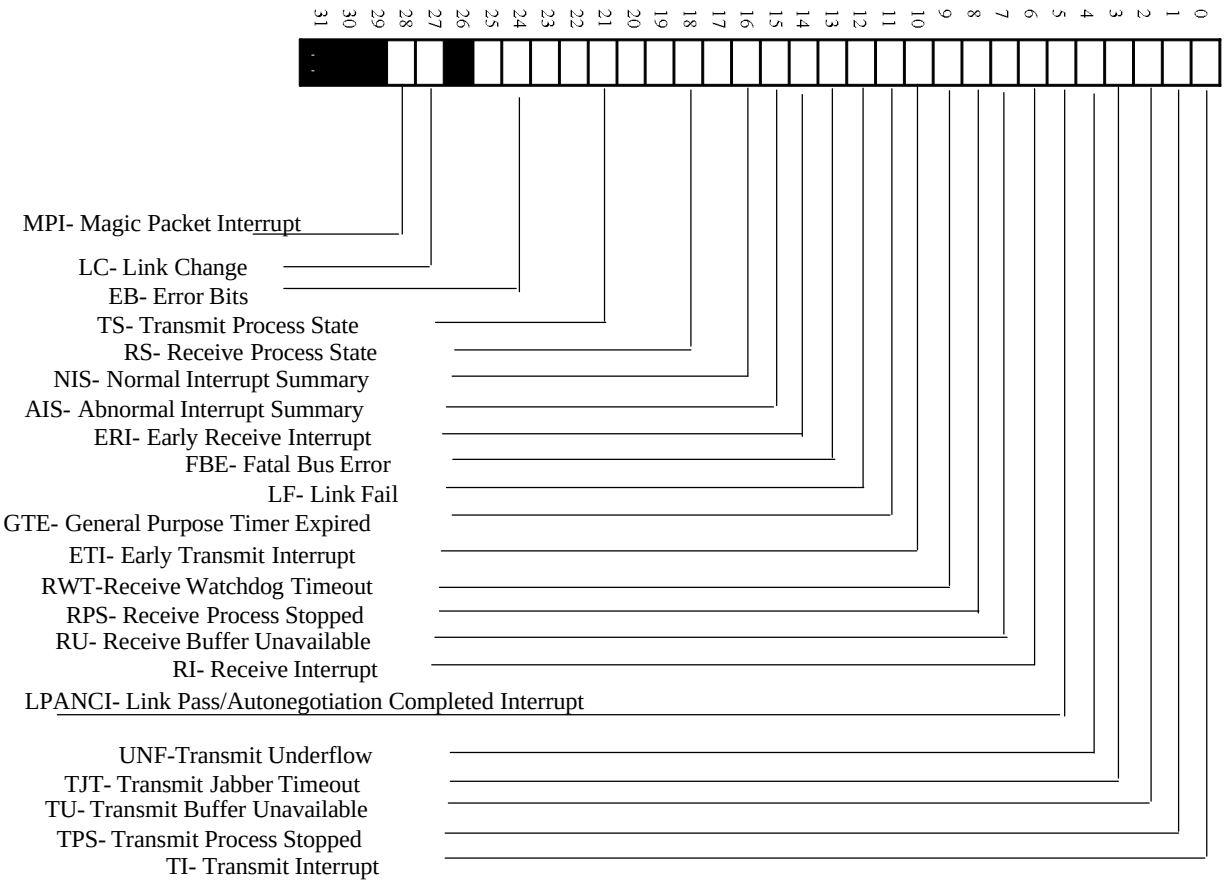
CSR3 Receive List Base Address



CSR4 Transmit List Base Address



5.2.5 STATUS REGISTER (CSR5)



Field	Name	Description
28	MPI	Magic packet received interrupt. Valid only if CSR16<22> bit is set.
27	LC	100 Base-TX link status has changed either from pass to fail or fail to pass. Read CSR12<1> for 100 Base-TX link status.
25:23	EB	Error Bits, read only, indicating the type of error that casued fatal bus error.
22:20	TS	Transmit Process State, read only bits indicating the state of transmit process.
19:17	RS	Receive Process State, read only bits indicating the state of receive process.
16	NIS	Normal Interrupt Summary, is the logical OR of CSR5<0>, CSR5<2> and CSR5<6> and CSR5<28>.
15	AIS	Abnormal Interrupt Summary, is the logical OR of CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CAR5,10>, CSR5<11> and CSR5<13>, CSR5<27>

14	ERI	Early receive interrupt, indicating the first buffer has been filled in ring mode, or 64 bytes has been received in chain mode.
13	FBE	Fatal Bus Error, indicating a system error occured, MX98713A will disable all bus access.
12	LF	Link Fail, indicates a link fail state in 10 Base-T port. This bit is valid only when CSR6<18>=0, CSR14<8>=1, and CSR13<3>=0.
11	GTE	General Purpose Timer Expired, indicating CSR11 counter has expired.
10	ETI	Early Transmit Interrupt, indicating the packet to be transmitted was fully transferred to internal TX FIFO. CSR5<0> will automatically clears this bit.
9	RWT	Receive Watchdog Timeout, reflects the network line status where receive watchdog timer has expired while the other node is still active on the network.
8	RPS	Write only, when written with any value, MX98713A reads receive descriptor list in host memory pointed by CSR4 and processes the list.
7	RU	Receive Buffer Unavailable, the receive process is suspended due to the next descriptor in the receive list is owned by host. If no receive poll command is issued, the reception process resumes when the next recognized incoming frame is received
6	RI	Receive Interrupt, indicating the completion of a frame reception.
5	UNF	Transmit Underflow, indicating transmit FIFO has run empty before the completion of a packet transmission.
4	LPANCI	When autonegotiation is not enabled (CSR14<7>=0), this bit indicates that the 10 Base-T link integrity test has completed successfully. After the link was down, this bit is also set as a result of writing 0 to CSR14<12> (Link Test Enable). When Autonegotiation is enabled (CSR14<7> =1) , this bit indicates that the autonegotiation has completed (CSR12<14:12>=5). CSR12 should then be read for a link status report. This bit is only valid when CSR6<18>=0, i.e. 10 Base-T port is selected Link Fail interrupt (CSR5<12>) will automatically clear this bit.
3	TJT	Transmit Jabber Timeout, indicating the MX98713A has been excessively active. The transmit process is aborted and placed in the stopped state. TDES0<1> is also set.
2	TU	Transmit Buffer Unavailable, transmit process is suspended due to the next descriptor in the transmit list is owned by host.
1	TPS	Transmit Process Stopped.
0	TI	Transmit Interrupt. indicating a frame transmission was completed.

TABLE 5.2.1 FATAL BUS ERROR BITS

CSR5<25:23>	Process State
000	parity error for either SERR# or PERR#, cleared by software reset.
001	master abort
010	target abort
011	reserved
1XX	reserved

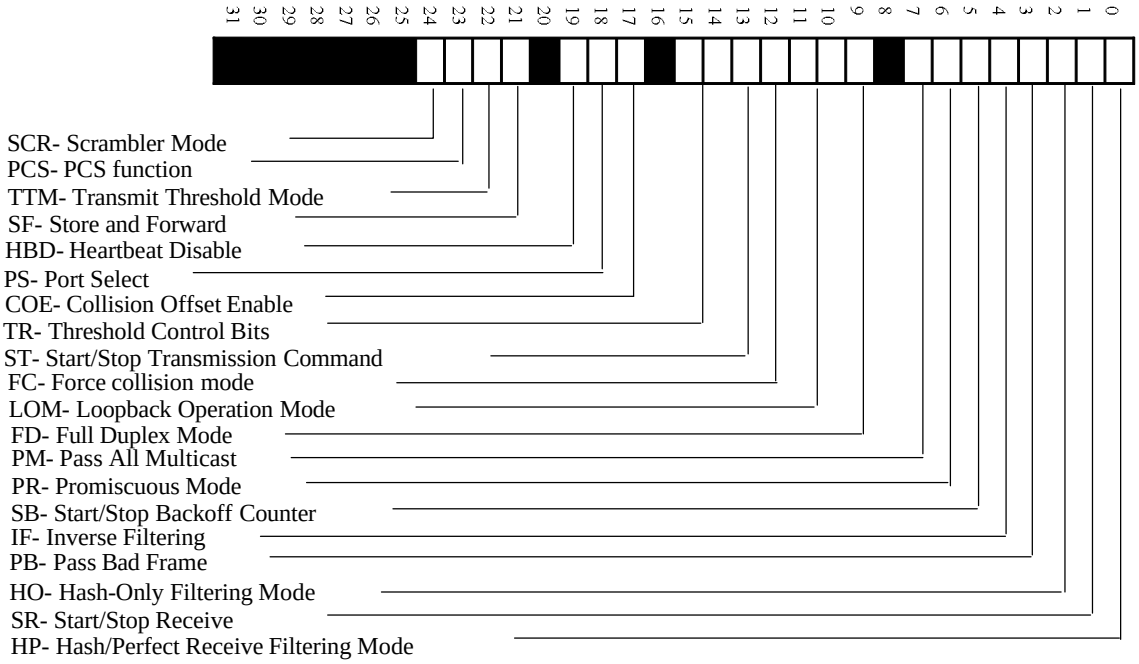
TABLE 5.2.2 TRANSMIT PROCESS STATE

CSR5<22:20>	Process State
000	stopped- reset or transmit jabber expired.
001	fetching transmit descriptor
010	waiting for end of transmission
011	filling transmit FIFO
100	reserved
101	Setup packet
110	Suspended, either FIFO underflow or unavailable transmit descriptor
111	closing transmit descriptor

TABLE 5.2.3 RECEIVE PROCESS STATE

CSR5<19:17>	Process State
000	stopped- reset or stop receive command
	fetching receive descriptor
010	checking for end of receive packet
011	waiting for receive packet
100	suspended, receive buffer unavailable
101	closing receive descriptor
110	Purging the current frame from the receive FIFO due to unavailable receive buffer
111	queuing the receive frame from the receive FIFO into host receive buffer

5.2.6 OPERATION MODE REGISTER (CSR6)



Field	Name	Description
24	SCR	Scrambler Mode, default is set to enable scrambler function. Not affected by software reset.
23	PCS	Default is set to enable PCS functions. CSR6<18> must be set in order to operate in symbol mode.
22	TTM	Transmit Threshold Mode, set for 10 Base-T and reset for 100 Base-TX.
21	SF	Store and Forward, when set, transmission starts only if a full packet is in transmit FIFO. the threshold values defined in CSR6<15:14> are ignored
19	HBD	Heartbeat Disable, set to disable SQE function in 10 Base-T mode.
18	PS	Port Select, deafult is o which is 10 Base-T mode, set for 100 Base-TX mode. A software reset does not affect this bit.
17	COE	Collision Offset Enable, set to enable a modified backoff algorithm during low collision situation, reset for normal backoff algorithm.
15:14	TR	Threshold Control Bits, these bits controls the selected threshold level for MX98713A's transmit FIFO, transmission starts when frame size within the transmit FIFO is larger than the selected threshold. Full frames with a length less than the threshold are also

transmitted.

13	ST	Start/Stop Transmission Command, set to place transmission process in running state and will try to transmit current descriptor in transmit list. When reset, transmit process is placed in stop state.
12	FC	Force Collision Mode, used in collision logic test in internal loopback mode, set to force collision during next transmission attempt. This can result in excessive collision reported in TDES0<8> if 16 or more collision.
11:10	LOM	Loopback Operation Mode, see table.
9	FD	Full-Duplex Mode, set for simultaneous transmit and receive operation, heartbeat check is disabled, TDES0<7> should be ignored, and internal loopback is not allowed. This bit controls the value of bit 6 of link code word .
7	PM	Pass All Multicast, set to accept all incoming frames with a multicast destination address are received. Incoming frames with physical address are filtered according to the CSR6<0> bit.
6	PR	Promiscuous Mode, any incoming valid frames are accepted, default is reset and not affected by software reset.
5	SB	Start/Stop Backoff Counter, when reset, the backoff timer is not affected by the network carrier activity. Otherwise, timer will start counting when carrier drops.
4	IF	Inverse Filtering, read only bit, set to operate in inverse filtering mode, only valid during perfect filtering mode.
3	PB	Pass Bad Frames, set to pass bad frame mode, all incoming frames passed the address filtering are accepted including runt frames, collided fragments, truncated frames caused by FIFO overflow.
2	HO	Hash-Only Filtering Mode , read only bit, set to operate in imperfect filtering mode for both physical and multicast addresses.
1	SR	Start/Stop Receive, set to place receive process in running state where descriptor acquisition is attempted from current position in the receive list. Reset to place the receive process in stop state.
0	HP	Hash/Perfect Receive Filtering Mode, read only bit, set to use hash table to filter multicast incoming frames. If CSR6<2> is also set, then the physical addresses are imperfect address filtered too. If CSR6<2> is reset, then physical addresses are perfect address filtered, according to a single physical address as specified in setup frame.

TABLE 5.2.4 TRANSMIT THRESHOLD

CSR6<21>	CSR6<15:14>	CSR6<22>=0 (for 100 Base-TX)	CSR6<22>=1 (Threshold bytes) (for 10 Base-T)
0	00	128	72

0	01	256	96
0	10	512	128
0	11	1024	160
1	XX	(Store and Forward)	

TABLE 5.2.5 DATA PORT SELECTION

CSR14<7>	CSR6<18>	CSR6<22>	CSR6<23>	CSR6<24>	Port
1	0	X	X	X	Nway Auto-negociation
0	0	1	X	X	10 Base-T
0	1	0	1	1	100 Base-TX

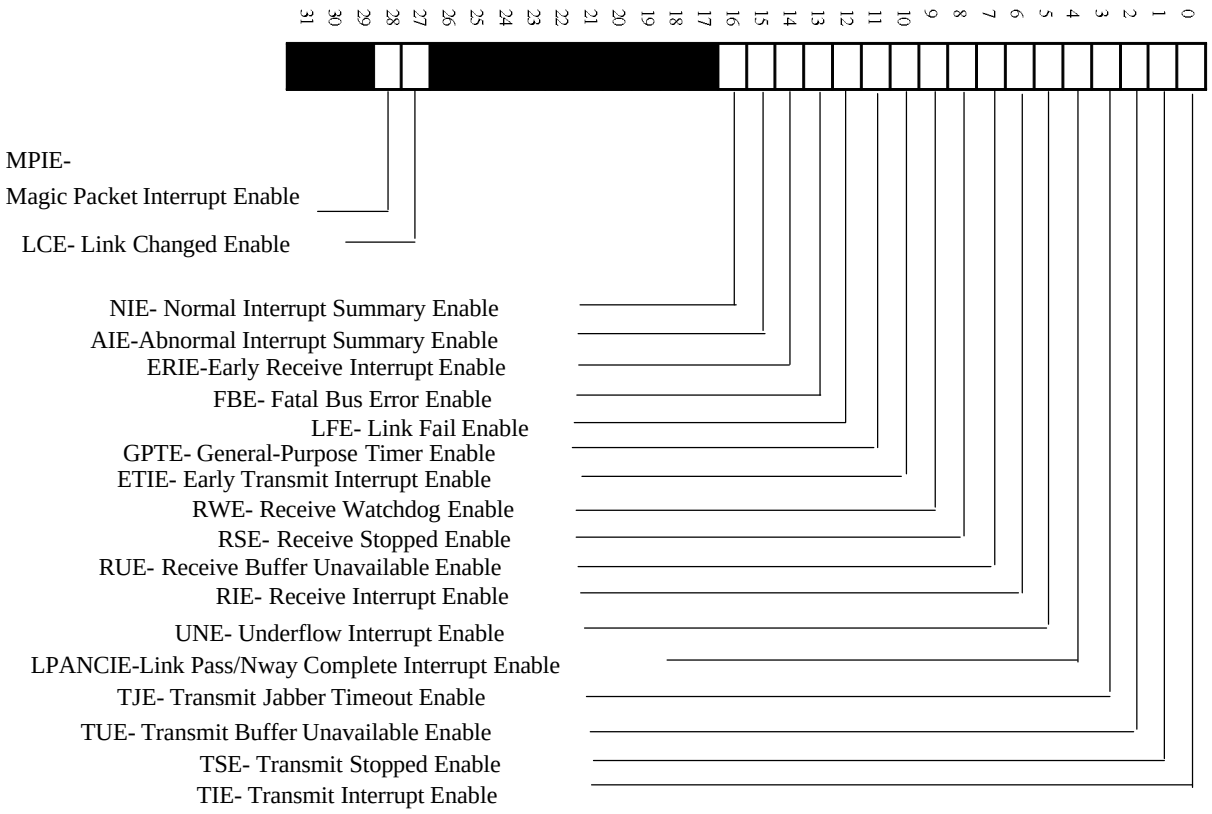
TABLE 5.2.6 LOOPBACK OPERATION MODE

CSR6<11:10>	Operation Mode
00	Normal
01	Internal loopback at FIFO port
11	Internal loopback at the PHY level
10	External loopback at the PMD level

TABLE 5.2.7 FILTERING MODE

CSR6<7>	CSR6<6>	CSR6<4>	CSR6<2>	CSR6<0>	Filtering Mode
0	0	0	0	0	16 perfect filtering
0	0	0	0	1	512-bit hash + 1 perfect filtering
0	0	0	1	1	512-bit hash for multicast and physical addresses
0	0	1	0	0	Inverse filtering
X	1	0	0	X	Promiscuous
0	1	0	1	1	Promiscuous
1	0	0	0	X	Pass All Multicast
1	0	0	1	1	Pass All Multicast

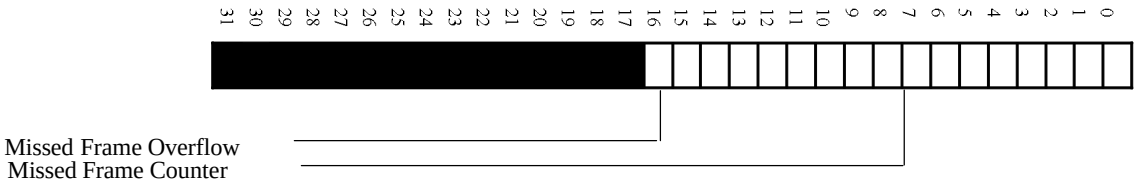
5.2.7 INTERRUPT MASK REGISTER (CSR7)



Field	Name	Description
28	MPIE	Magic Packet Interrupt Enable, enables CSR5<28>.
27	LCE	Link Changed Enable, enables CSR5<27>.
16	NIE	Normal Interrupt Summary Enable, set to enable CSR5<0>, CSR5<2>, CSR5<6>.
15	AIE	Abnormal Interrupt Summary enable, set to enbale CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CSR5<11> and CSR5<13>.
14	ERIE	Early Receive Interrupt Enable
13	FBE	Fatal Bus Error Enable, set together with with CSR7<15> enables CSR5<13>.
12	LFE	Link Fail Interrupt Enable, enables CSR5<12>
11	GPTE	General_-Purpose Timer Enable, set together with CSr7<15> enables CSR5<11>.
10	ETIE	Early Transmit Interrupt Enable, enables CSR5<10>
9	RWE	Receive Watchdog Timeout Enable, set together with CSR7<15> enables CSR5<9>.
8	RSE	Receive Stopped Enable, set together with CSR7<15> enables CSR5<8>.

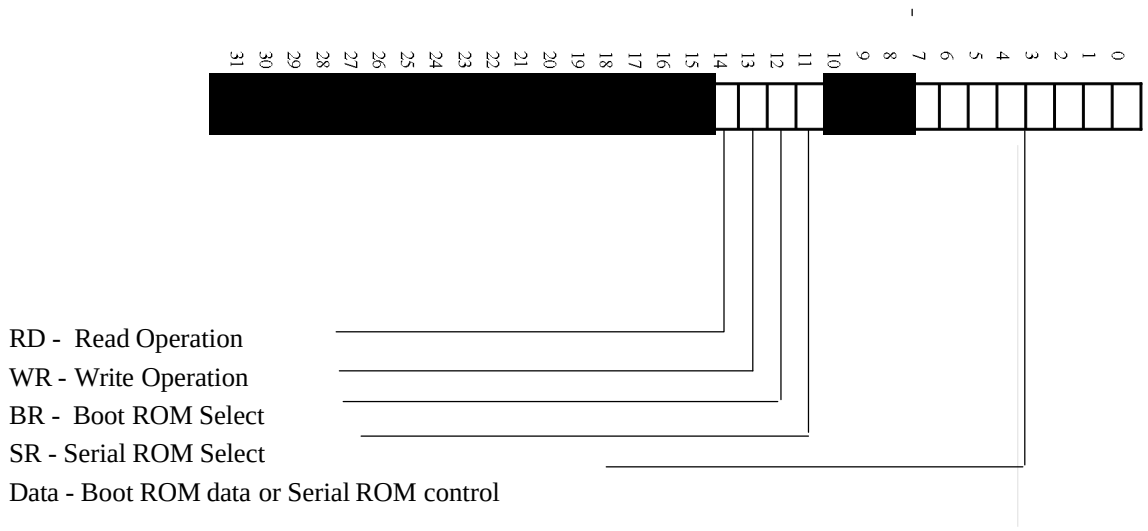
7	RUE	Receive Buffer Unavailable Enable, set together with CSR7<15> enables CSR5<7>.
6	RIE	Receive Interrupt Enable, set together with CSR7<16> enables CSR5<6>.
5	UNE	Underflow Interrupt Enable, set together with CSR7<15> enables CSR5<5>.
4	LPANCIE	Link Pass/Autonegotiation Completed Interrupt Enable
3	TJE	Transmit Jabber Timeout Enable, set together with CSR7<15> enables CSR5<3>.
2	TUE	Transmit Buffer Unavailable Enable, set together with CSR7<16> enables CSR5<2>.
1	TSE	Transmit Stop Enable, set together with CSR7<15> enables CSR5<1>.
0	TIE	Transmit Interrupt Enable, set together with CSR7<16> enables CSr5<0>.

5.2.8 MISSED RAME COUNTER (CSR8)



Field	Name	Description
16	MFO	Missed Frame Overflow, set when missed frame counter overflows, reset when CSR8 is read.
15:0	MFC	Missed Frame Counter, indicates the number of frames discarded because no host receive descriptors were available.

5.2.9 NON-VOLATILE MEMORY CONTROL REGISTER (CSR9)



Field	Name	Description
14	RD	Boot ROM read operation when boot ROM is selected.
13	WR	Boot ROM write operation when boot ROM is slected.
12	BR	Boot ROM Select, set to select boot ROM only if CSR9<11>=0.
11	SR	Serial ROM Select, set to select serial ROM for either read or write operation.
7:0	Data	If boot ROM is selected (CSR9<12> is set), this field contains the data to be read from and written to the boot ROM. If serial ROM is selected , CSR9<3:0> are defined as follows :
		3 SDO Serial ROM data out from serial ROM into MX98713A.
		2 SDI Serial ROM data input to serial ROM from MX98713A.
		1 SCLK Serial clock output to serial ROM.
		0 SCS Chip select output to serial ROM.

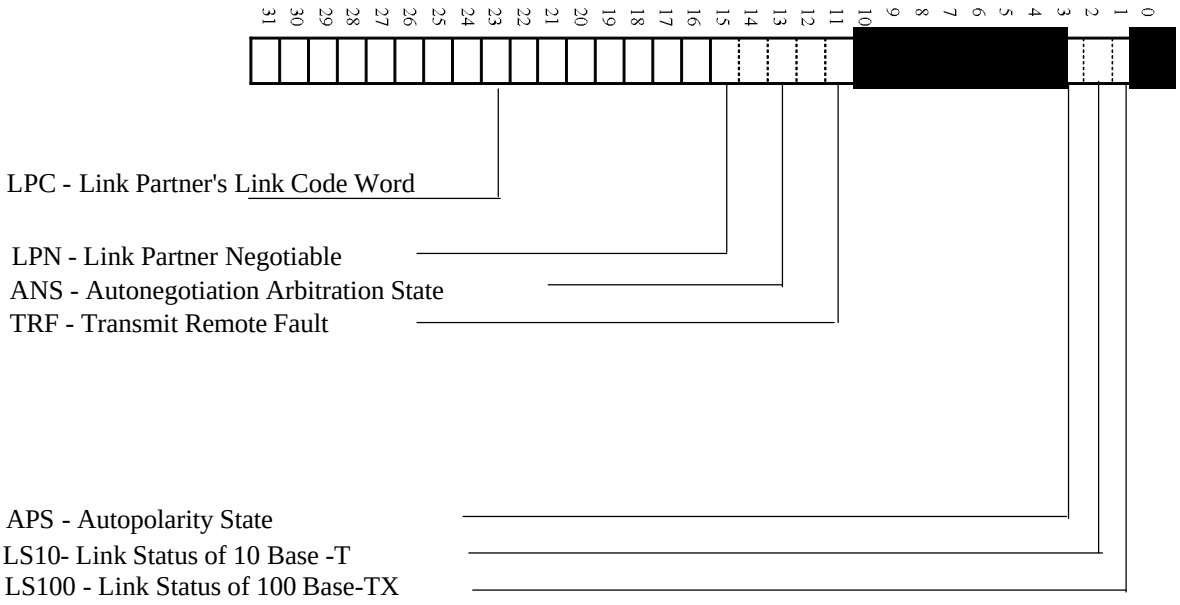
Warning : CSR9<11> and CSR9<12> should be mutually exclusive for correct operations.

5.2.10 FLASH MEMORY PROGRAMMING ADDRESS REGISTER (CSR10)

5.2.11 GENERAL PURPOSE TIMER (CSR11)

Field	Name	Description
16	CON	When set,the general purpose timer is in continuous operating mode. When reset, the timer is in one-shot mode.
15:0	Timer	Value contains the timer value in a cycle time of 204.8us.

5.2.12 10 BASE-T STATUS PORT (CSR12)

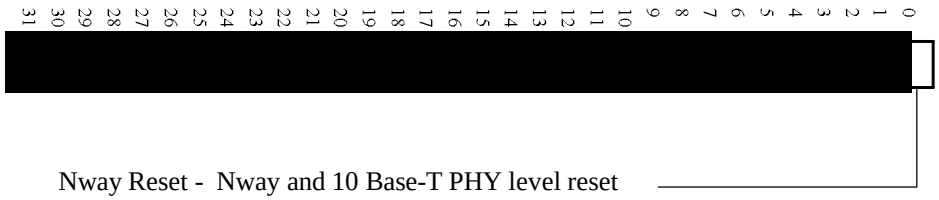


* Software reset has no effect on this register

Field	Name	Decription
31:16	LPC	Link Partner's Link Code Word, where bit 16 is S0 (selector field bit 0) and bit 31 is NP (Next Page). Effective only when CSR12<15> is read as a logical 1. the following field.
15	LPN	Link Partner Negotiable, set when link partner support NWAY algorithm and CSR14<7> is set.
14:12	ANS	Autonegotiation Arbitration State, arbitration states are defined 000 = Autonegotiation disable 001 = Transmit disable 010 = ability detect 011 = Acknowledge detect 100 = Complete acknowledge detect 101 = FLP link good; autonegotiation complete 110 = Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated, write 001 into this field can restart the autonegotiation sequence if CSR14<7> is set. Oth

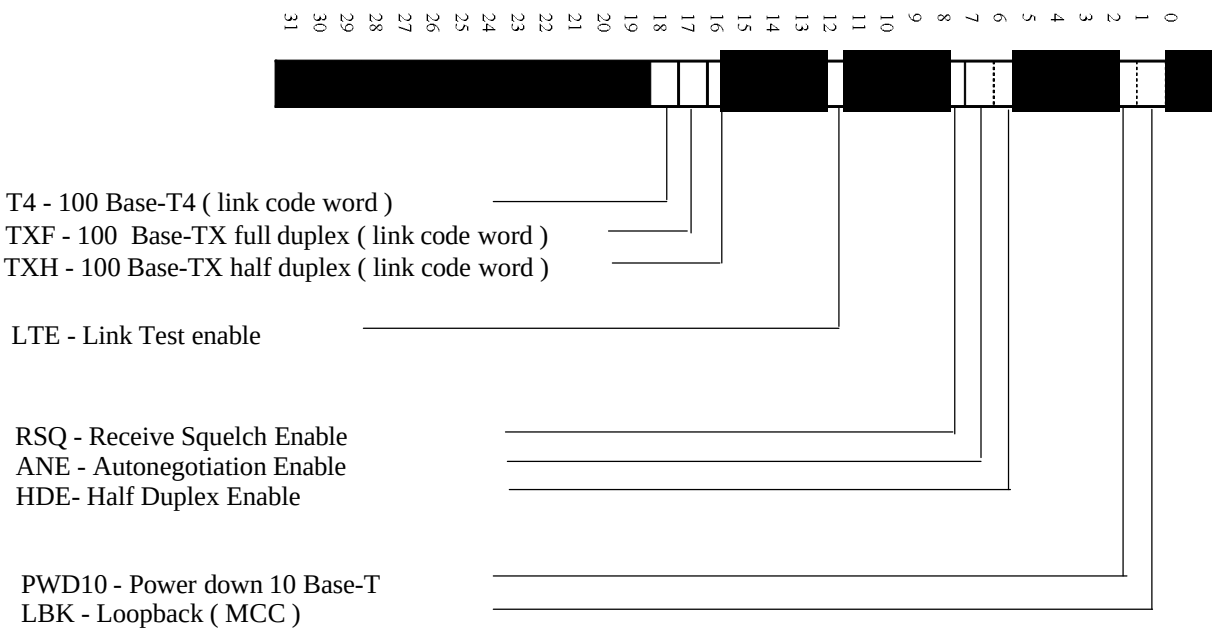
		erwise, these bits should be 0.
11	TRF	Transmit Remote Fault
3	APS	Autopolarity State, set when polarity is positive. When reset, the 10Base-T polarity is negative. The received bit stream is inverted by the receiver.
2	LS10	Set when link status of 10 Base-T port link test fail. Reset when 10 Base-T link test is in pass state.
1	LS100	Link state of 100 Base-TX, this bit reflects the state of SD pin, effective only when CSR6<23>= 1 (PCS is set). Set to indicate a fail condition .i.e. SD=0.

5.2.13 SIA RESET REGISTER (CSR13)



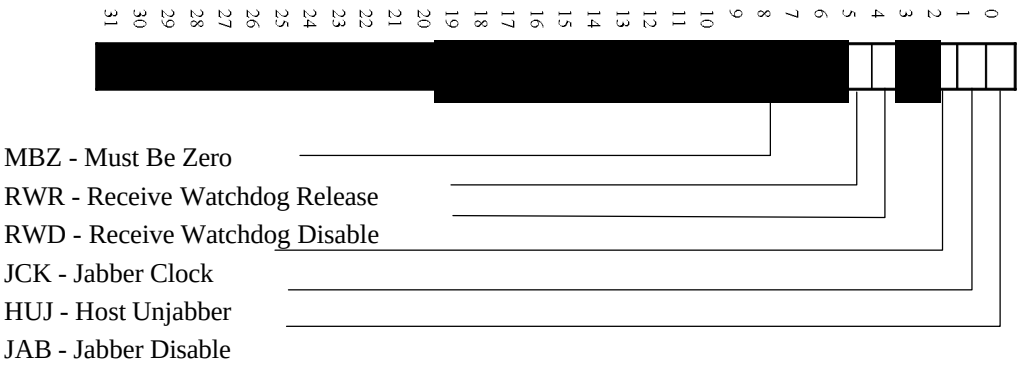
Field	Name	Decription
0	Nway Reset	While writing 0 to this bit, resets the CSR12 & CSR14.

5.2.14 10 BASE-T CONTROL PORT (CSR14)



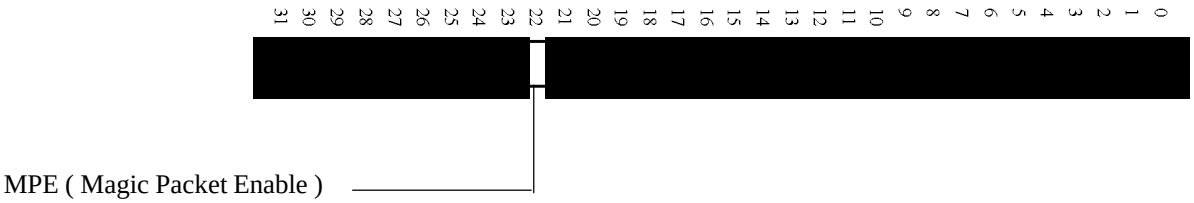
Field	Name	Decription
18	T4	Bit 9 of link code word for T4 mode.
17	TXF	Bit 8 of link code word for 100 Base-TX full duplex mode.
16	TXH	Bit 7 of link code word for 100 Base-TX half duplex mode. Meaningful only when CSR14<7> (ANE) is set.
12	LTE	Link Test Enable, when set the 10 Base-T port link test function is enabled.
8	RSQ	Receive Squelch Enable for 10 Base-T port. Set to enable.
7	ANE	Autonegotiation Enable, .
6	HDE	Half-Duplex Enable, this is the bit 5 of link code word, only meaningful when CSR14<7> is set.
2	PWD10	set to power down 10 Base-T module, this will force both TX and RX port into tri-state and prevent AC current path. Reset for normal 10 Base-T operation.
1	LBK	Loop back enable for 10 Base-T MCC.

5.2.15 WATCHDOG TIMER (CSR15)



Field	Name	Description
5	RWR	Defines the time interval no carrier from receive watchdog expiration until reenabling the receive channel. When set, the receive watchdog is release 40-48 bit times from the last carrier deassertion. When reset, the receive watchdog is released 16 to 24 bit times from the last carrier deassertion.
4	RWD	When set, the receive watchdog counter is disable. When reset, receive carriers longer than 2560 bytes are guaranted to cause the watchdog counter to time out. Packets shorter than 2048 bytes are guaranted to pass.
2	JCK	When set, transmission is cut off after a range of 2048 bytes to 2560 bytes is tranmitted. When reset, transmission for the 10 Base-T port is cut off after a range of 26 ms to 33ms. When reset, transmission for the 100 Base-TX port is cut off after a range of 2.6ms to 3.3ms.
1	HUJ	Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the jabber is released 365ms to 420 ms after jabber expiration for 10 Base-T port. When reset, the jabber is released 36.5ms to 42ms after the jabber exporation for 100 Base-TX port.
0	JBD	Jabber Disable, set to disable transmit jabber function.

5.2.16 MAGIC PACKET REGISTER (CSR16)

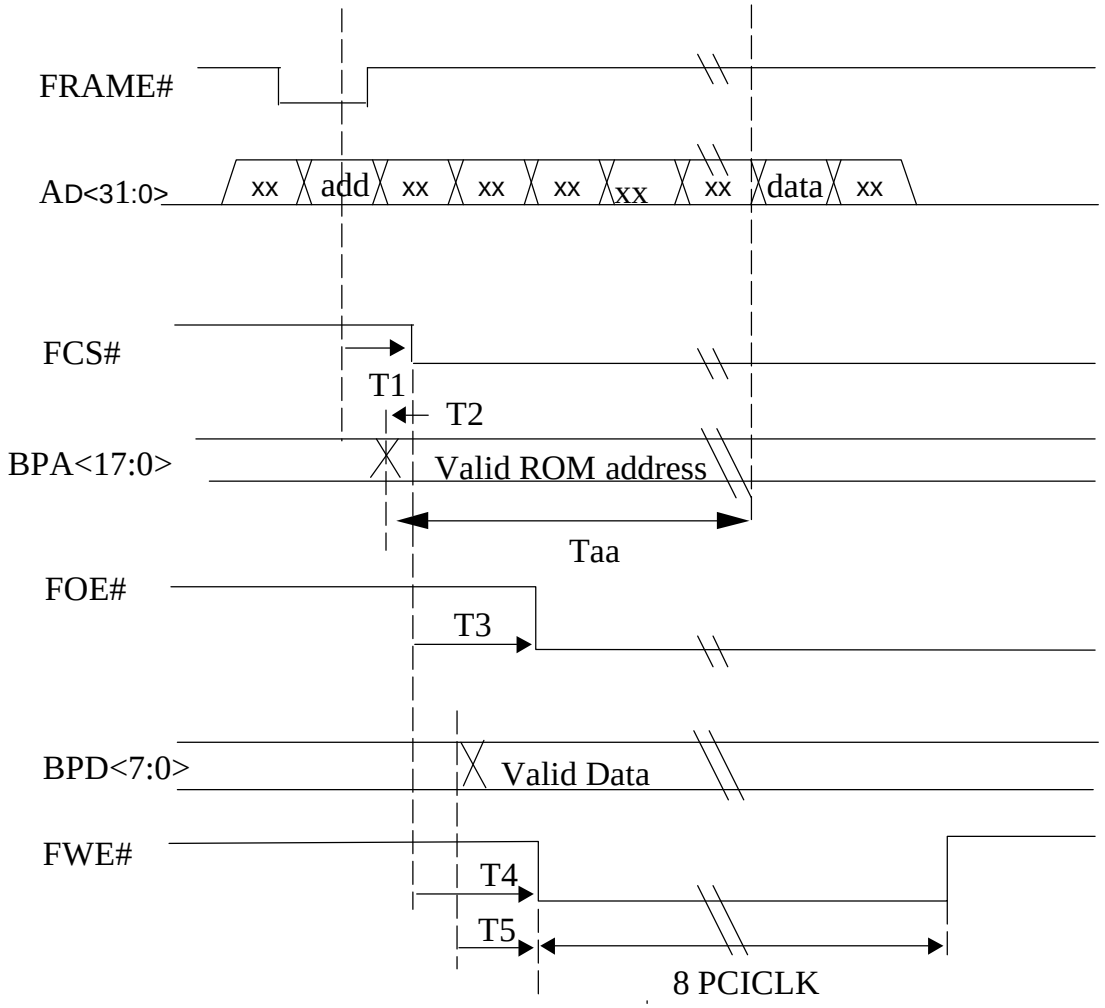


field	Name	Description
bit 31:23	reserved	
bit 22	MPE	Magic Packet Enable, set to enable Magic Packet Mode
bit 21:0	reserved	

Sleep mode and MPE mode can be used seperately. When Sleep and MPE are both set, the Sleep mode dominate MPE, i.e., no magic packet can be detected since both TX and RX channel are shut off in sleep mode. In both sleep and Magic Packet mode, PWD100B will be asserted low to shut down external 100 Base-TX PHY/PMD chips. On the detection of magic packet, PWD100B pin will be asserted high.

6. AC/DC CHARACTERISTICS

6.1 BOOT ROM AND FLASH TIMING



-PCI adddress to FCS# valid delay T1 < 1 PCICLK
-BPA address valid to CS# low >= 0 ns
-Boot ROM speed grade (Taa) <= 8 PCICLK - 15 ns
e.g. For 33MHz PCI bus, Taa <= 225ns, T1 <= 90ns
-FCS# low till FOE# low (T3) >= 2 PCICLK
-FCS# low till FWE# low (T4) >= 0ns
-Data valid till FWE# low (T5) >= 0ns

6.2 ABSOLUTE OPERATION CONDITION

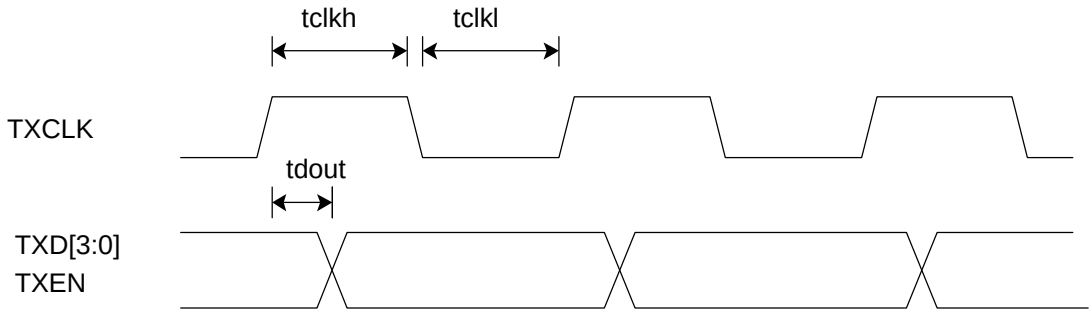
Supply Voltage (VCC)	-0.5V to +7.0V
DC Input Voltage (Vin)	-0.5V to VCC + 0.5V
DC Output Voltage (Vout)	-0.5V to VCC + 0.5V
Storage Temperature Range (Tstg)	-55°C to +150°C
Power Dissipation (PD)	TBD
Lead Temp. (TL) (Soldering, 10 sec)	260°C
ESD Rating (Rzap = 1.5k, Czap = 100pF)	1.5kV
Clamp Diode Current	$\pm$20mA

6.3 DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Units
TTL/PCI Input/Output					
Voh	Minimum High Level Output Voltage	Ioh = -3mA	2.4		V
Vol	Maximum Low Level Output Voltage	Iol = +6mA		0.4	V
Vih	Minimum High Level Input Voltage		2.0		V
Vil	Maximum Low Level Input Voltage			0.8	V
Iin	Input Current	Vi = VCC or GND	- 1.0	+ 1.0	uA
Ioz	Minimum TRI-STATE Output Leakage Current	Vout = VCC or GND	-10	+10	uA
LED output Driver					
Vlol	LED turn on Output Voltage	Iol = 16mA		0.4	V
Supply					
Idd	Average Supply Current	CKREF =25MHz PCICLK = 33MHz	TBD	TBD	mA
Vdd	Average Supply Voltage		4.75V	5.25V	V

7.0 AC CHARACTERIZATION

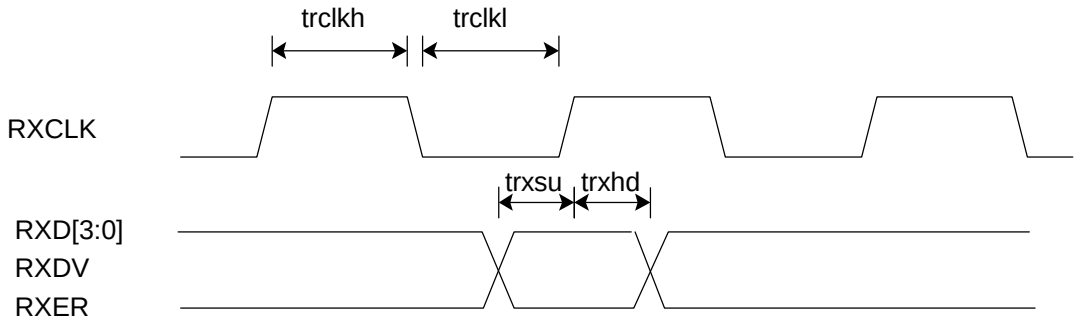
7.1 TRANSMIT SIGNAL TIMING:



Symbol	Parameter	Min	Max	Units
tclkh	TXCLK high for 25MHz (100 Base-TX)	14	26	ns
	TXCLK high for 2.5MHz (10 Base-T)	140	260	ns
tclkl	TXCLK low for 25MHz (100 Base-TX)	14	26	ns
	TXCLK low for 2.5MHz (10 Base-T)	140	260	ns
tdout	TXD,TXEN to TXCLK rising edge	2	25	ns

* The duty cycle of the TXCLK signal shall be between 35% and 65% inclusively.

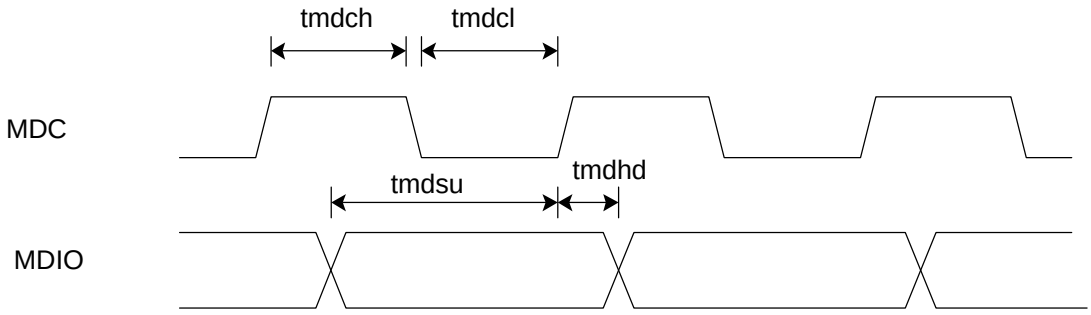
7.2 RECEIVE SIGNNAL TIMING



Symbol	Parameter	Min	Max	Units
trclkh**	RXCLK high for 25MHz (100 Base-TX)	14	26	ns
	RXCLK high for 2.5MHz (10 Base-T)	140	260	ns
trclkl**	RXCLK low for 25MHz (100 Base-TX)	14	26	ns
	RXCLK low for 2.5MHz (10 Base-T)	140	260	ns
trxsu	RXD,RXDV & RXER setup time to RXCLK rising edge	10		ns
trxhd	RXD,RXDV & RXER hold time to RXCLK rising edge	10		ns

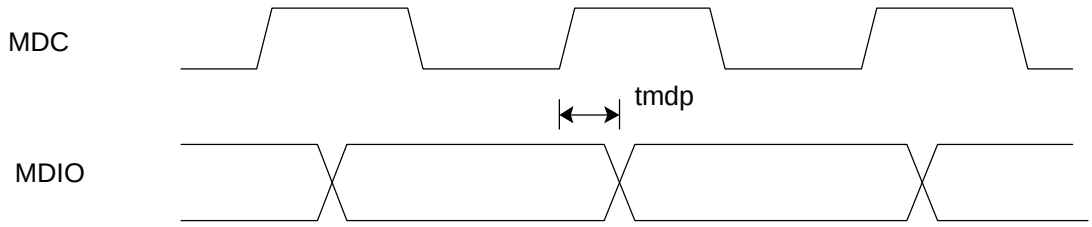
* The maximun time of 10Base-T is not guaranteed at begginning and end of frame.
* The minimun high and low times of RXCLK shall be 35% of the nominal period.

7.3 Management Signal Timing MDIO source by STA(station management entity):



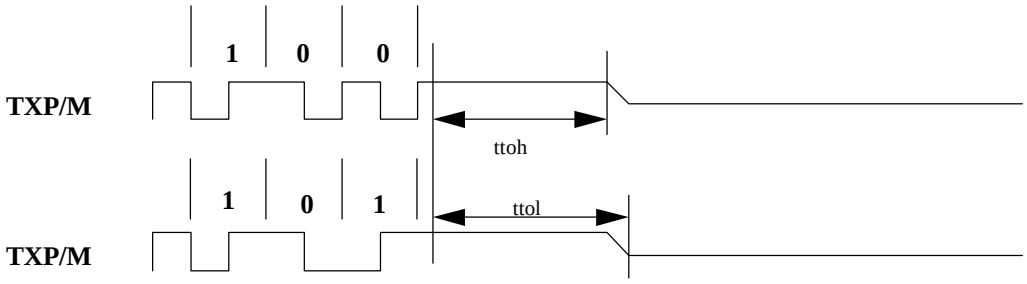
Symbol	Parameter	Min	Max	Units
tmdch	MDC high time	200		ns
tmdcl	MDC low time	200		ns
tmdsu	MDIO to MDC high setup time sourced by STA	10		ns
tmdhd	MDIO to MDC high hold time sourced by STA	10		ns

7.4 MANAGEMENT SIGNAL TIMING MDIO SOURCE BY PHY:



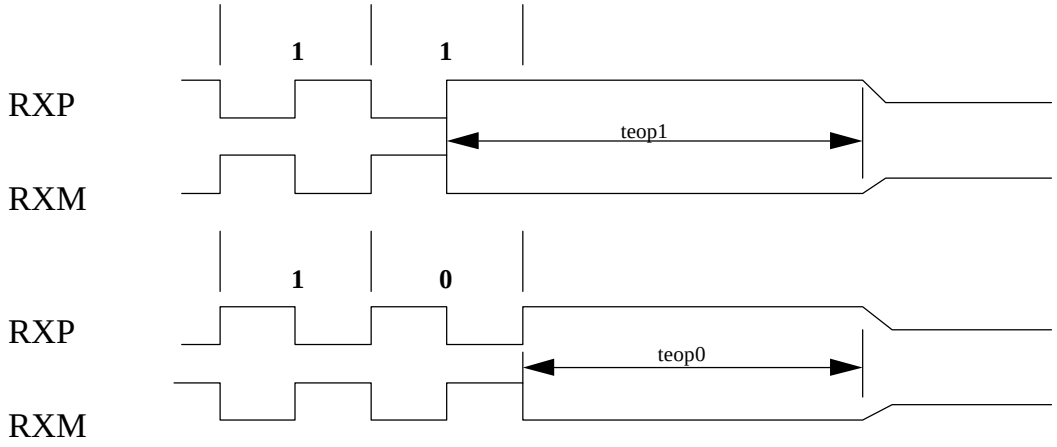
Symbol	Parameter	Min	Max	Units
tmdp	MDC high to MDIO data valid	2	300	ns

7.5 10BASE-T TRANSMIT TIMING (End of Packet)



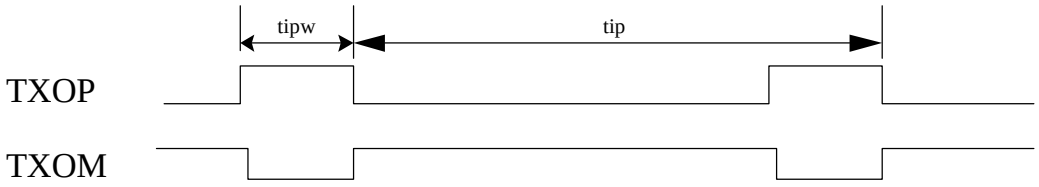
Symbol	Parameter	Min	Max	Units
ttoh	Transmit Output High before Idle (Half Step)	200		ns
ttol	Transmit Output Idle Time (Half Step)		800	ns

7.6 10BASE-T RECEIVE END OF PACKET TIMING



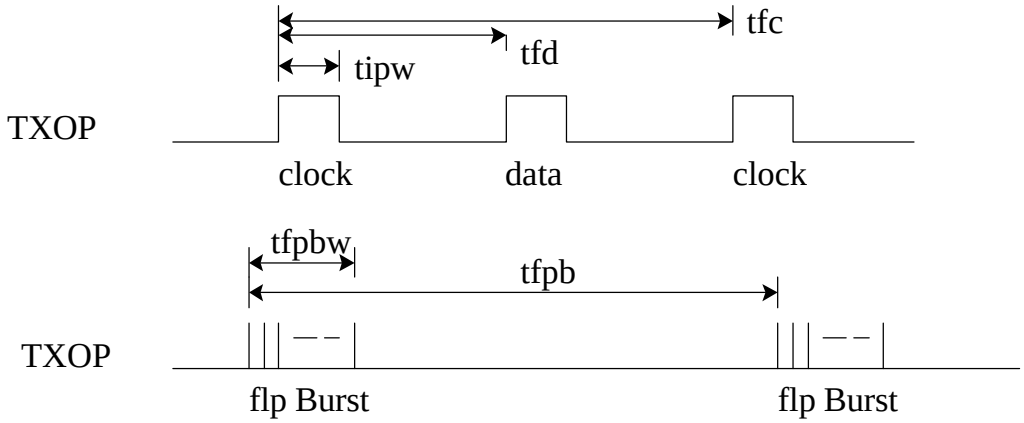
Symbol	Parameter	Min	Max	Units
teop1	Receive End of Packet Hold Time after "1"	225		ns
teop0	Receive End of Packet Hold time after "0"	225		ns

7.7 10BASE-T LINK PULSE TIMING



Symbol	Parameter	Min	Max	Units
tip	Time between Link Output Pulses	8	24	ms
tipw	Link Integrity Output Pulse Width	80	130	ns

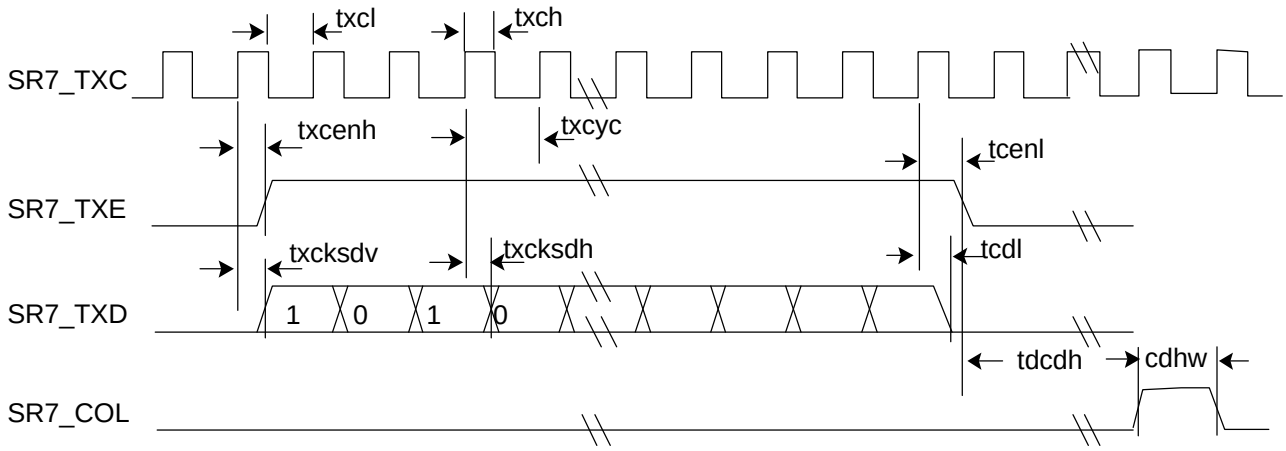
7.8 FLP (Fast Link Pulse) TIMING:



Symbol	Parameter	Min	Max	Units
tfd	Flp Clock Pulse to Data Pulse (Data = 1)	58	65	us
tfc	Flp Clock Pulse to Clock Pulse	118	130	us
tipw	Fast Link Output Pulse Width	80	130	ns
tfpb	FLP burst to FLP Burst	12	18	ms
tfpbw	FLP Burst Width	1.8	2.1	ms

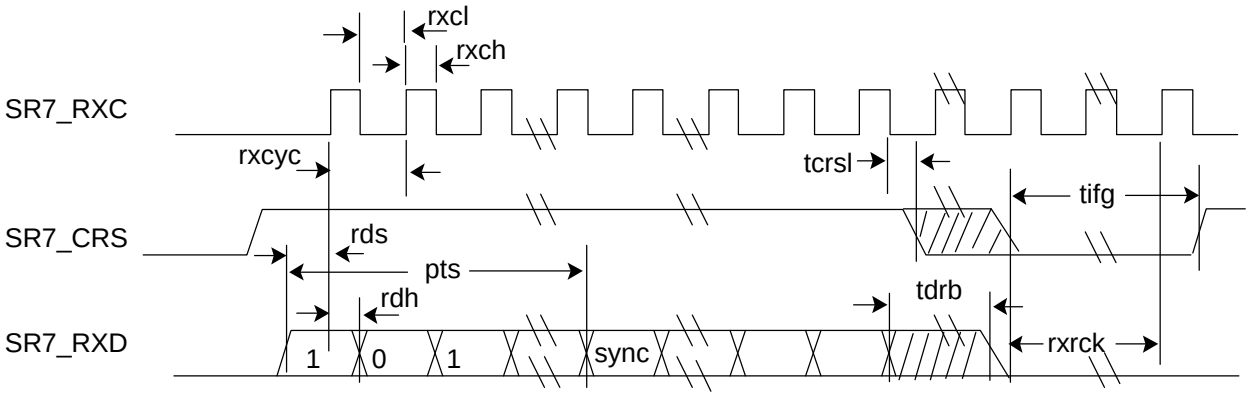
Note: FLP related timing parameters are guranted by design and not measured data on tester.

7.9 SERIAL TRANSMISSION WITH A COLLISION DETECT HEARTBEAT TIMING



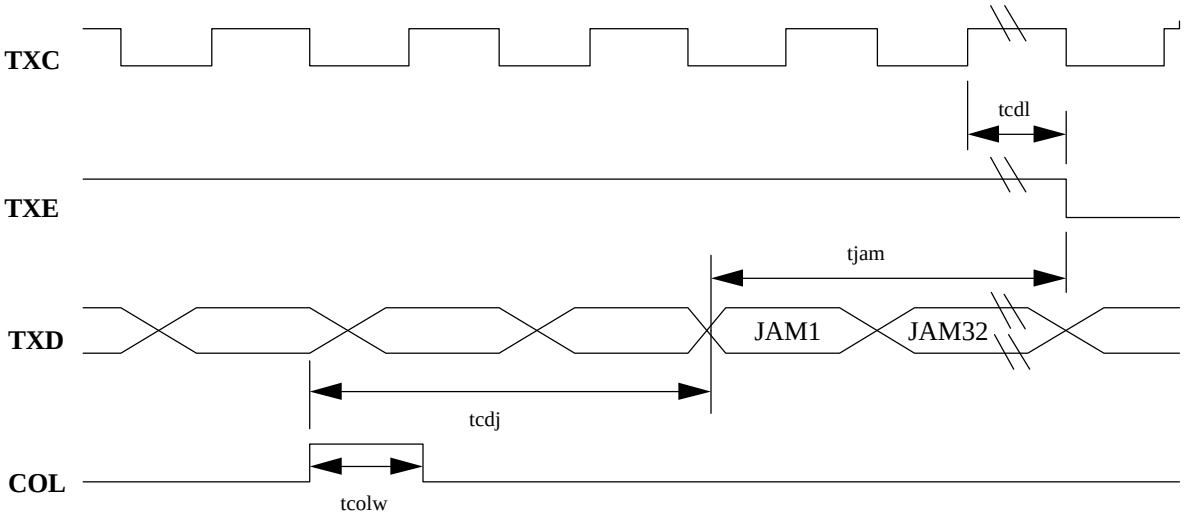
Symbol	Parameter	Min	Max	Units
txch	Transmit Clock High Time	36		ns
txcl	Transmit Clock Low Time	36		ns
txcyc	Transmit Clock Cycle Time	90	1100	ns
txcenh	Transmit Clock High to Transmt Enable High		45	ns
txcksdv	Transmit Clock High to Serial Data Valid		65	ns
txcksdh	Serial Data Hold Time from Transmit Clock High	6		ns
tcdl	Transmit Clock to Data Low		55	ns
tcenl	Transmit Clock to SR7_TXE Low		55	ns
tdcdh	SR7_TXE Low to Start of Collision Dectect Heartbeat	0	64	txcyc
cdhw	Collision Dectect Width	2		txcyc

7.10 SERIAL RECEIVE TIMING DIAGRAM



Symbol	Parameter	Min	Max	Units
rxch	Receive Clock High Time	36		ns
rxcl	Receive Clock Low Time	36		ns
rxcyc	Receive Clock Cycle Time	90	1100	ns
rds	Receive Data Setup Time to Receive Clock High	20		ns
rdh	Receive Data Hold Time from Receive Clock High	15		ns
pts	First Preamble Bit to Synchronize	8		rxcyc
rxrck	Minimun Number of Receive Clocks after CRS Low	3		rxcyc
tdrb	Maximun of Allowed Dribble Bits/Clocks		5	rxcyc
tifg	Receive Recovery Time		40	rxcyc
tcrsl	Receive Clock to Carrier Sense Low	0	1	rxcyc

7.11 SERIAL TRANSMIT TIMING DIAGRAM



Symbol	Parameter	Min	Max	Units
tcolw	Collision Detect Width	2		txcyc cycles
tcdj	Delay From Collision to First Bit of JAM (Note 1)		8	txcyc cycles
tjam	JAM Period (Note 2)		32	txcyc cycles

Note 1 : The NIC must synchronize to collision detect. If the NIC is in the middle of serializing a byte of data the remainder of the byte will be serialized. Thus the jam pattern will start anywhere from 1 to 8 TXC cycles after COL is asserted.

Note 2 : The NIC always issues 32 bits of jam. The jam is all 1's data.

8.0 PACKAGE INFORMATION

160-PIN PLASTIC QUAD FLAT PACK

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MACRONIX INTERNATIONAL CO., LTD. reserves the right to change product and specifications without notice.