TC9021

PCI 10/100/1000 Ethernet MAC Controller

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PCI 10/100/1000 Ethernet MAC Controller

1 Features

PCI & DMA Features

PCI Specification Revision 2.2 compliant
64-bit, 33/66MHz bus master capability
Efficient DMA operation maximizes PCI band-width utilization
1 Terabyte (40 bit) address space
Scatter, gather transmit/receive DMA
Transmit "interrupt-less" mode of operation
Transmit frame priority queuing
Receive frame priority interrupts
Receive interrupt coalescing

FIFO Features

Large transmit & receive FIFO
No external memory required
Receive FIFO flow control thresholds

MAC Features

IEEE 802.3z, 802.3x compliant
IEEE 802.1p, 802.1Q compliant
1000Mbps, 100Mbps, 10Mbps triple speed, half/full duplex operation
Transmit and receive back to back frames at full wire speed
Half duplex carrier extension and packet burst-ing
Asymmetric/symmetric flow control
VLAN tag insertion/removal
VLAN tagged frame filtering
IP, TCP, UDP checksum calculation/verification
802.3 MIB & RMON MIB statistic register sets
64-bit hash table for multicast frame filtering
Jumbo frame support, transmit and receive
GMII and MII support

1000BASE-X PCS Features

For use with 1000BASE-X Gigabit PHY devices having Ten Bit Interface (TBI)
8B10B encoder/decoder
Auto-Negotiation
PHY management registers

Power Management

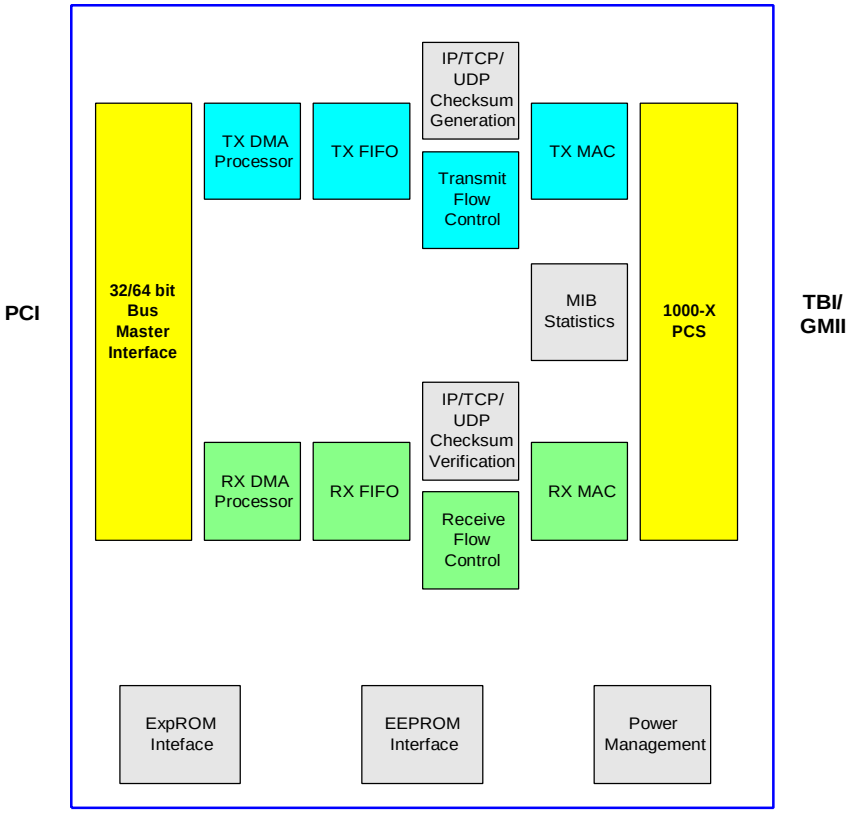
WakeOnLAN support
ACPI Revision 1.0 compliant
2.5/3.3V CMOS with 5V tolerant I/O
Low power 0.25µm technology
208-pin PQFP

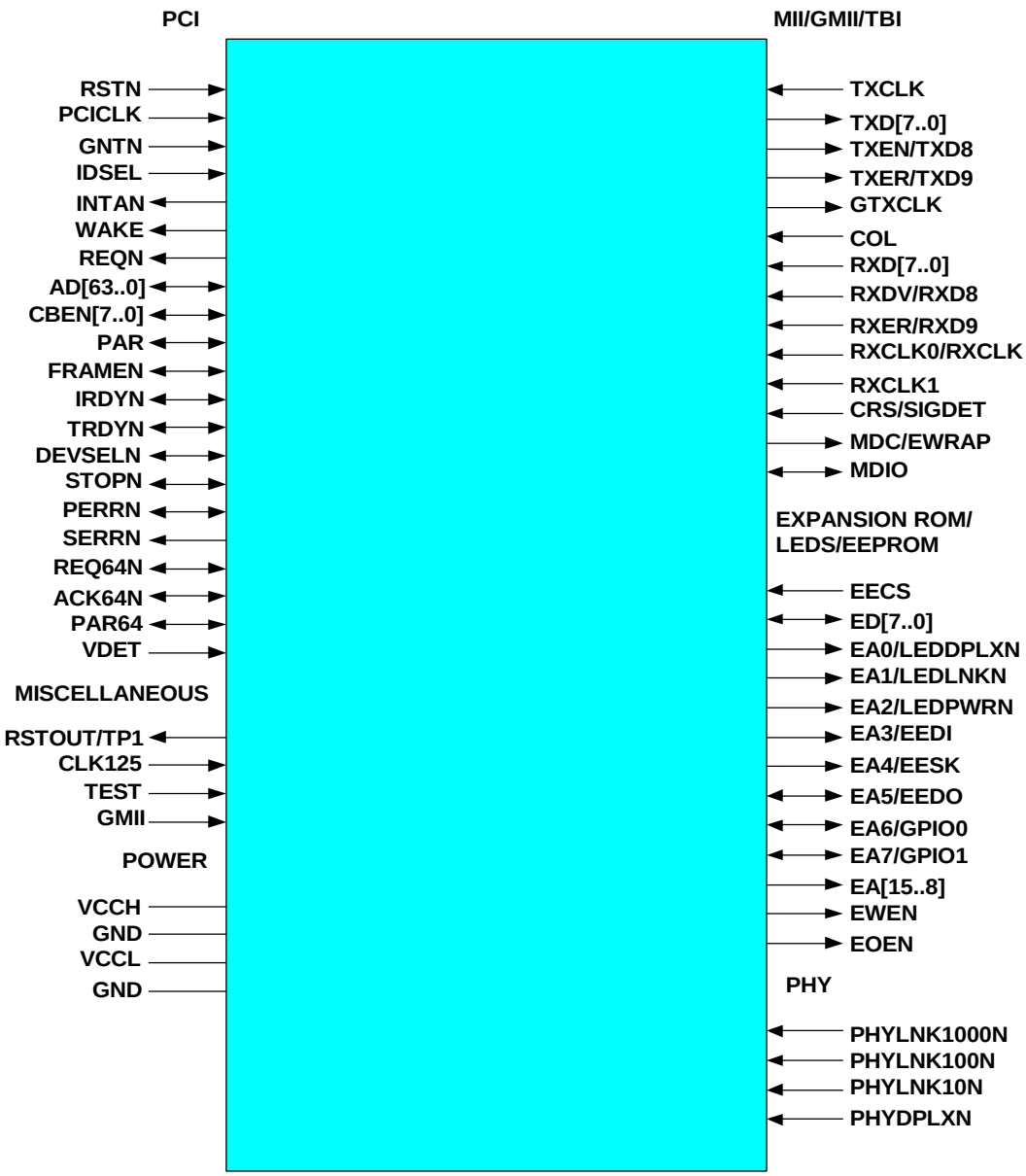
2 General Description

The TC9021 is designed as a high performance, host-optimized network interface, targeted for applications (either embedded or as a standard NIC) operating in full or half duplex Gigabit Ether-net LANs.
The highly efficient scatter/gather DMA logic moves data between 1 terabyte of system memory via the 64-bit 66MHz PCI bus interface. After the DMA processing overhead, each independent transmit and receive DMA channel can sustain well over 1 gigabit per second of throughput. The TC9021 stores frames in large integrated data buffers, eliminating the need for external buffer memory.

In order to reduce the processing load of the host CPU, the TC9021 implements TCP, UDP and IP V4 checksum generation and validation. A flexible scheme to coalesce host system interrupts allows the host CPU to process multiple frames with a single interrupt from the TC9021, further increasing the efficiency of the host system.
The TC9021 supports 802.1p/Q tagged frames by automatically inserting and removing the tag fields, which allows for compatibility with legacy hardware and software. Receive tagged frames can be filtered by the device according to the VLAN ID of the frame. The arrival of higher priority frames can be programmed to generate immediate interrupts for notification to the host system.
The TC9021 supports jumbo frame technology that allows for extension of Ethernet frame length up to 9018 (or 9022 for VLAN tagged) octets. Tests have shown servers using jumbo frames has significant performance improvement over non-jumbo frame enabled systems when operating in a Gigabit Ethernet environment.
The TC9021 is compliant to 802.3x Full Duplex standard, and supporting both symmetrical and asymmetrical flow control. PAUSE frames can be automatically generated by the device according to programmable flow control thresholds associated with the receive buffer.
To support half duplex gigabit operation, the TC9021 inplements carrier extension and packet bursting functions compliant to 802.3z standard.
The TC9021 supports three PHY interfaces, the standard media independent MII (for 10Mbps and 100Mbps PHY) and GMII (for 1000Mbps PHY), and the defacto TBI interface for 1000BASE-X PHY.
To further optimize the system configuration for 1000BASE-X systems, the TC9021 implements the entire 1000BASE-X PCS function, including 8B10B encoder and decoder, and Auto-Negotiation. The TBI interface allows the TC9021 to be connected directly to an industry standard SERDES device for 1000BASE-X applications.
The TC9021 is fully compliant with ACPI Power Management specification revision 1.0. The TC9021 also supports Wake-On-LAN and Magic Packet power management remote wakeup mechanisms.
The TC9021 implements a complete set of Ether-net management statistic MIB and RMON counters that provide detail performance information about the network and the interface.

3 Block Diagram





4 Pin Designations

TABLE 1: TC9021 Pin Designations

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
1	MDIO	53	AD17	105	VCCH	157	ED5
2	MDC/EWRAP	54	AD16	106	AD62	158	ED4
3	CRS/SIGDET	55	VCCH	107	AD61	159	ED3
4	COL	56	CBEN2	108	AD60	160	VCCH
5	GND	57	FRAMEN	109	AD59	161	ED2
6	GTXCLK	58	IRDYN	110	GND	162	ED1
7	VCCH	59	GND	111	AD58	163	ED0
8	TXER/TXD9	60	TRDYN	112	AD57	164	EA0/LEDDPLXN
9	TXEN/TXD8	61	DEVSELN	113	AD56	165	EA1/LEDLNK1000N
10	TXD7	62	STOPN	114	VCCH	166	GND
11	TXD6	63	PERRN	115	AD55	167	EA2/LEDPWRN
12	TXD5	64	VCCH	116	AD54	168	EA3/EEDI
13	TXD4	65	SERRN	117	AD53	169	EA4/EESK
14	GND	66	PAR	118	GND	170	EA5/EEDO
15	TXD3	67	CBEN1	119	AD52	171	EA6/GPIO0
16	TXD2	68	GND	120	GND	172	PWRRSTN(VCCH)
17	TXD1	69	GND	121	AD51	173	EA7/GPIO1
18	GND	70	AD15	122	VCCL	174	GND
19	TXD0	71	VCCL	123	AD50	175	EA8
20	VCCL	72	AD14	124	AD49	176	EA9
21	TXCLK	73	AD13	125	VCCH	177	EA10
22	WAKE	74	AD12	126	AD48	178	EA11
23	INTAN	75	VCCH	127	AD47	179	EA12
24	RSTN	76	AD11	128	GND	180	EA13
25	VCCH	77	AD10	129	AD46	181	VCCL
26	PCICLK	78	GND	130	AD45	182	EA14/LEDLNK100N
27	GND	79	AD9	131	AD44	183	EA15/LEDLNK10N
28	GNTN	80	AD8	132	AD43	184	GND
29	REQN	81	CBEN0	133	AD42	185	CLK125
30	AD31	82	AD7	134	VCCH	186	VCCH
31	AD30	83	AD6	135	AD41	187	TEST
32	AD29	84	VCCH	136	GND	188	GMII
33	GND	85	VCCL	137	GND	189	RSTOUT
34	GND	86	AD5	138	AD40	190	GND
35	AD28	87	GND	139	VCCL	191	PHYDPLXN
36	VCCL	88	GND	140	AD39	192	PHYLNK10N
37	VCCH	89	AD4	141	AD38	193	PHYLNK100N
38	AD27	90	AD3	142	AD37	194	PHYLNK1000N
39	AD26	91	AD2	143	AD36	195	RXD0
40	AD25	92	AD1	144	VCCH	196	RXD1

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
41	AD24	93	AD0	145	AD35	197	RXD2
42	CBEN3	94	GND	146	GND	198	RXD3
43	GND	95	ACK64N	147	AD34	199	RXD4
44	IDSEL	96	VCCH	148	AD33	200	RXD5
45	AD23	97	REQ64N	149	AD32	201	RXD6
46	VCCH	98	CBEN7	150	VDET	202	RXD7
47	AD22	99	CBEN6	151	EECS	203	RXDV/RXD8
48	AD21	100	CBEN5	152	EWEN	204	RXER/RXD9
49	AD20	101	CBEN4	153	EOEN	205	GND
50	AD19	102	GND	154	GND	206	RXCLK0/RXCLK
51	GND	103	PAR64	155	ED7	207	VCCH
52	AD18	104	AD63	156	ED6	208	RXCLK1

5 Signal Descriptions

TABLE 2: TC9021 Signal Descriptions

PCI		
Signal Name	**Signal Type**	**Signal Description**
RSTN	INPUT	**Reset, asserted LOW.** RSTN will cause the TC9021 to reset all of its functional blocks. RSTN must be asserted for a minimum duration of 10 PCICLK cycles.
PCICLK	INPUT	**PCI Bus Clock.** This clock is used to drive the PCI bus interfaces and the internal DMA logic. All bus signals are sampled on the rising edge of PCICLK. PCICLK can operate from 0MHz to 66MHz.
GNTN	INPUT	**PCI Bus Grant, asserted LOW.** GNTN signals access to the PCI bus has been granted to the device.
IDSEL	INPUT	**Initialization Device Select.** The ISEL is used to select the TC9021 during configuration read and write transactions.
INTAN	OUTPUT	**Interrupt Request, asserted LOW.** The TC9021 asserts INTAN to request an interrupt, when any one of the programmed interrupt event occurs.
WAKE	OUTPUT	**Wake Event, assertion level is programmable.** The TC9021 asserts WAKE to signal the detection of a wake event. The WAKE signal eventually drives the PCI bus PME# signal, but is not intended to be directly connected to PME#. See the PCI Bus Power Management Interface Specification for details on generating PME# from WAKE.
REQN	OUTPUT	**Request, asserted LOW.** The TC9021 asserts REQN to request PCI bus master operation.
AD[63..0]	IN/OUT	**PCI Bus Address/Data.** Address and data are multiplexed on the AD pins. Bits 0 through 31 carry the lower 32 bits of the physical address during the first clock cycle of a transaction, and carry data during the subsequent clock cycles. Bits 32 through 63 carry the upper 32 bits of the physical address during the first clock cycle of a transaction (if the Dual Address Cycle, or DAC command is used along with the assertion of REQ64N), and carry an additional 32 bits of data during subsequent clock cycles (if a 64 bit transaction has been

PCI		
Signal Name	**Signal Type**	**Signal Description**
		negotiated through the assertion of both REQ64N and ACK64N).
CBEN[7..0]	IN/OUT	**PCI Bus Command/Byte Enable, asserted LOW.** Bus command and byte enables are multiplexed on the CBEN signals. CBEN specify the bus command during the address phase transaction, and carry byte enables during the data phase. CBEN bits 4 through 7 are reserved unless a 64 bit transaction has been negotiated through the assertion of both REQ64N and ACK64N.
PAR	IN/OUT	**Parity.** PCI Bus parity is even across bits 0 through 31 of AD and bits 0 through 3 of CBEN. The TC9021 generates PAR during address and write data phases as a bus master, and during read data phase as a target. It checks for correct parity during read data phase as bus master, during every address phase as a bus slave, and during write data phases as a target.
FRAMEN	IN/OUT	**PCI Bus Cycle Frame, asserted LOW.** FRAMEN is asserted at the beginning of the address phase of the bus transaction and deasserted before the final transfer of the data phase of the transaction.
IRDYN	IN/OUT	**Initiator Ready, asserted LOW.** A bus master asserts IRDYN to indicate valid data phases on AD during write data phases, and to indicate it is ready to accept data during read data phases. A target will monitor IRDYN.
TRDYN	IN/OUT	**Target Ready, asserted LOW.** A bus target asserts TRDYN to indicate valid read data phases, and to indicate it is ready to accept data during write data phases. A bus master will monitor TRDYN.
DEVSELN	IN/OUT	**Device Select, asserted LOW.** The TC9021 asserts DEVSELN when it is selected as a target during a bus transaction. It monitors DEVSELN for any target to acknowledge a bus transaction initiated by the device.
STOPN	IN/OUT	**Stop, asserted LOW.** STOPN is driven by the slave target to inform the bus master to terminate the current transaction.
PERRN	IN/OUT	**Parity Error, asserted LOW.** The TC9021 asserts PERRN when it checks and detects a bus parity errors. When it is generating PAR output, the device monitors for any reported parity error on PERRN.
SERRN	OUTPUT	**System Error, asserted LOW.**
REQ64N	IN/OUT	**64 Bit Transaction Request, asserted LOW.** The REQ64N signal is asserted by a bus master to indicate a preference for 64 bit transaction.
ACK64N	IN/OUT	**64 Bit Transaction Acknowledgment, asserted LOW.** The ACK64N signal is asserted by a bus target which supports 64 bit transactions in response to REQ64N assertion.
PAR64	IN/OUT	**Parity.** PCI Bus parity is even across bits 32 through 63 of AD and bits 4 through 7 of CBEN. The TC9021 generates PAR64 during address and write data phases as a bus master, and during read data phase as a target. It checks for correct parity during read data phase as bus master, during every address phase as a bus slave, and during write data phases as a target.
VDET	INPUT	**Power Detect.** The device detects PCI bus power supply loss when VDET is LOW.

MII/GMII/TBI		
Signal Name	**Signal Type**	**Signal Description**
TXCLK	INPUT	**Transmit Clock.** TXCLK is a continuous clock supplied by the PHY to synchronize transmit data transfers when the TC9021 is configured in 10Mbps or 100Mbps Mode. The nominal rate of TXCLK is 2.5MHz for 10Mbps operation, and 25MHz for 100Mbps operation.
TXD[7..0]	OUTPUT	**Transmit Data.** Eight bits of transmit data from the transmit MAC to the PHY device. When the TC9021 is configured in GMII Mode, these signals represent the entire transmit data bus. TXD are synchronized to the GTXCLK. When the TC9021 is configured in TBI Mode, these pins represent the lower 8 bits of the 10-bit transmit data bus. TXD are synchronized with GTXCLK.
TXEN/TXD8	OUTPUT	**Transmit Enable/Transmit Data Bit 9.** When the TC9021 is configured in GMII mode, this signal is TXEN. When asserted, TXEN/TXD8 indicates to the PHY that TXD carry valid transmit data. TXEN/TXD8 is asserted with the first byte of the preamble until the last byte of the frame data. When the TC9021 is configured in TBI Mode, this signal is TXD[8], the ninth transmit data bit. TXEN/TXD8 is synchronous with GTXCLK.
TXER/TXD9	OUTPUT	**Transmit Error/Transmit Data Bit 10.** When the TC9021 is configured in GMII mode, this signal is TXER. When asserted, TXER/TXD9 indicates to the PHY that an error symbol should be transmitted in place of the TXD transmit data. When the TC9021 is configured in TBI Mode, this signal is TXD[9], the tenth transmit data bit. TXER/TXD9 is synchronous with GTXCLK.
GTXCLK	OUTPUT	**Gigabit Transmit Clock.** GTXCLK is a continuous clock supplied to the PHY to synchronize transmit data transfers when the device is configured in GMII Mode or TBI Mode. The nominal rate of GTXCLK is 125MHz.
COL	INPUT	**Collision.** When the TC9021 is configured in TBI Mode, COL is ignored and should be tied LOW. When the TC9021 is configured in GMII Mode, COL is asserted by the PHY to signal a collision condition is detected on the physical medium. COL is asynchronous.
RXD[7..0]	INPUT	**Receive Data.** 8 bits of receive data from the PHY device to the receive MAC. When the TC9021 is configured in GMII Mode, these signals represent the entire receive data bus. In GMII Mode, RXD are synchronized to the RXCLK0/RXCLK. When the TC9021 is configured in TBI Mode, these pins represent the lower 8 bits of the 10-bit receive data bus. In TBI Mode, RXD are synchronized with both RXCLK0/RXCLK and RXCLK1.
RXDV/RXD8	INPUT	**Receive Data Valid/Receive Data Bit 9.** When the TC9021 is configured in GMII Mode, this signal is RXDV, indicating valid frame data is present on the RXD pins. The PHY asserts RXDV/RXD8 before the SFD, and de-asserts it after the last data nibble of the frame. In GMII mode, RXDV/RXD8 is synchronous with RXCLK0/RXCLK. When the TC9021 is configured in TBI Mode, this signal is RXD[8], the ninth receive data bit. In TBI mode, RXDV/RXD8 is synchronous with both RXCLK0/RXCLK and RXCLK1.
RXER/RXD9	INPUT	Receive Error/Receive Data Bit 10. When the TC9021 is configured in GMII Mode, this signal is RXER, an

MII/GMII/TBI		
Signal Name	**Signal Type**	**Signal Description**
		indication from the PHY that an error has been detected during frame data reception. In GMII mode, RXER/RXD9 is synchronous with **RXCLK0/RXCLK.** When the TC9021 is configured in TBI Bode, this signal is RXD[9], the tenth receive data bit. In TBI mode, RXER/RXD9 is synchronous with both RXCLK0/RXCLK and RXCLK1.
RXCLK0/RXCLK	INPUT	**Receive Clock Zero.** When the TC9021 is configured in GMII Mode, RXCLK0/RXCLK provide the timing reference for RXD, RXDV/RXD8, and RXER/RXD9 signals. The nominal rate for RXCLK0/RXCLK is 125MHz. When the TC9021 is configured in TBI Mode, RXCLK0/RXCLK and RXCLK1 together provide a timing reference for the 10-bit data bus defined by RXD, RXDV/RXD8, and RXER/RXD9 signals. RXDLK0/RXCLK rising edges correspond to odd-numbered code-groups appearing on the 10-bit data bus defined by RXD, RXDV/RXD8, and RXER/RXD9 signals. RXCLK0/RXCLK and RXCLK1 are supplied by the PHY based on the receive clock recovery circuit. RXCLK0/RXCLK and RXCLK1 are 180 degrees out of phase. Nominal rate for RXCLK0/RXCLK is 62.5MHz. RXCLK0/RXCLK may be stretched, but is never shortened.
RXCLK1	INPUT	**Receive Clock One.** When the TC9021 is configured in GMII Mode, RXCLK1 is ignored and should be tied LOW. When the TC9021 is configured in TBI mode, RXCLK0/RXCLK and RXCLK1 together provide a timing reference for the 10-bit data bus defined by RXD, RXDV/RXD8, and RXER/RXD9 signals. RXCLK1 rising edges correspond to even-numbered code-groups appearing on the 10-bit data bus defined by RXD, RXDV/RXD8, and RXER/RXD9 signal. RXCLK0/RXCLK and RXCLK1 are supplied by the PHY based on the receive clock recovery circuit. RXCLK0/RXCLK and RXCLK1 are 180 degrees out of phase. Nominal rate for RXCLK1 is 62.5MHz. RXCLK1 may be stretched, but is never shortened.
CRS/SIGDET	INPUT	**Carrier Sense/Signal Detect.** When the TC9021 is configured in GMII Mode, this signal is CRS, asserted by the PHY to signal a non-idle medium with either transmit or receive activity detected. CRS is asynchronous. When the TC9021 is configured in TBI Mode, this signal is SIGDET. An indication from the media transceiver that a signal is present.
MDC/EWRAP	OUTPUT	**Management Data Clock/Electrically Wrap.** When the TC9021 is configured in GMII Mode, this signal is MDC which is used to synchronize the read and write operations of MDIO. When the TC9021 is configured in TBI Mode, this signal is EWRAP which is asserted HIGH to indicate the PHY device should internally loop transmit data to the receiver, and should keep the transmitter serial outputs in a static state. MDC/EWRAP asserted LOW indicates the PHY device should operate normally.
MDIO	IN/OUT	Management Data Input/Output. When the TC9021 is configured in TBI Mode, MDIO is ignored and should be tied HIGH through a resistor (10kΩ or higher). When the device is configured in GMII Mode, MDIO carries management data for the management port read and write operations.

PHY INTERFACE		
Signal Name	**Signal Type**	**Signal Description**

PHY INTERFACE		
Signal Name	**Signal Type**	**Signal Description**
PHYLNK1000N	INPUT	**PHY Link 1000Mbps Status, asserted LOW.** PHYLNK1000N is driven by the physical layer device. It is asserted to signal a functional 1000Mbps link (link up).
PHYLNK100N	INPUT	**PHY Link 100Mbps Status, asserted LOW.** PHYLNK100N is driven by the physical layer device. It is asserted to signal a functional 100Mbps link (link up).
PHYLNK10N	INPUT	**PHY Link 10Mbps Status, asserted LOW.** PHYLNK10N is driven by the physical layer device. It is asserted to signal a functional 10Mbps link (link up).
PHYDPLXN	INPUT	**PHY Duplex Status, assertion level is programmable.** PHYDPLXN is driven by the physical layer device. It is asserted to indicate a full duplex link, and de-asserted to indicate a half duplex link. PHYDPLXN is undefined when PHYLNK10N is not asserted.

EEPROM INTERFACE(SEE ALSO EXPANSION ROM INTERFACE/LED DRIVERS)		
Signal Name	**Signal Type**	**Signal Description**
EECS	OUTPUT	EEPROM Chip Select. EECS is asserted by the TC9021 to access the EEPROM. EECS is connected directly to the chip select input of the EEPROM device.

EXPANSION ROM INTERFACE/LED DRIVERS		
Signal Name	**Signal Type**	**Signal Description**
ED[7..0]	IN/OUT	**Expansion ROM Data.** ED provide data access to the expansion ROM.
EA15/LEDLNK10N	OUTPUT	**Expansion ROM Address Bit 15/10Mbps Link Status LED.** EA15/LEDLNK10N is a shared pin assuming the value of bit 15 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddre and ExpRomData registers). If the expansion ROM is not being accessed, EA15/LEDLNK10N is the 10Mbps Link Status LED driver signal.
EA14/LEDLNK100N	OUTPUT	**Expansion ROM Address Bit 14/100Mbps Link Status LED.** EA14/LEDLNK100N is a shared pin assuming the value of bit 14 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accessed, EA14/LEDLNK100N is the 100Mbps Link Status LED driver signal.
EA[13..8]	OUTPUT	**Expansion ROM Address.** The EA along with EA7/GPIO1, EA6/GPIO0, EA5/EEDO, EA4/EESK, EA3/EEDI, EA2/LEDPWRN, EA1/LEDLNK1000N, and EA0/LEDDPLXN carry the address to the expansion ROM.
EA7/GPIO1	IN/OUT	**Expansion ROM Address Bit 7/General Purpose Input/Output 1.** EA7/GPIO1 is a shared pin assuming the value of bit 7 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accessed, EA7/GPIO1 is the general purpose input/output bit 1.
EA6/GPIO0	IN/OUT	**Expansion ROM Address Bit 6/General Purpose Input/Output 0.** EA6/GPIO0 is a shared pin assuming the value of bit 6 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accessed, EA6/GPIO0 is the general purpose input/output bit 0.

EXPANSION ROM INTERFACE/LED DRIVERS		
Signal Name	**Signal Type**	**Signal Description**
EA5/EEDO	IN/OUT	Expansion ROM Address Bit 5/EEPROM Data Output. EA5/EEDO is a shared pin assuming the value of bit 5 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accessed, EA5/EEDO is an input connected directly to the data output of the EEPROM device.
EA4/EESK	OUTPUT	**Expansion ROM Address Bit 4/EEPROM Serial Clock.** EA4/EESK is a shared pin assuming the value of bit 4 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accessed, EA4/EESK is the clock (frequency 150kHz) used to synchronize the EEPROM data access with EA3/EEDI and EA5/EEDO. EA4/EESK is connected directly to the clock input of the EEPROM device.
EA3/EEDI	OUTPUT	**Expansion ROM Address Bit 3/EEPROM Data Input.** EA3/EEDI is a shared pin assuming the value of bit 3 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accessed, EA3/EEDI is the data input to an EEPROM. EA3/EEDI is connected directly to the data input of the EEPROM device.
EA2/LEDPWRN	OUTPUT	**Expansion ROM Address Bit 2/Power Status LED.** EA2/LEDPWRN is a shared pin assuming the value of bit 2 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accesses, EA2/LEDPWRN is the Power Status LED driver signal.
EA1/LEDLNK1000N	OUTPUT	**Expansion ROM Address Bit 1/1000Mbps Link Status LED.** EA1/LEDLNK1000N is a shared pin assuming the value of bit 1 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accesses, EA1/LEDLNK1000N is the 1000Mbps Link Status LED driver signal.
EA0/LEDDPLXN	OUTPUT	**Expansion ROM Address Bit 0/Power Status LED.** EA0/LEDDPLXN is a shared pin assuming the value of bit 0 of the expansion ROM address during accesses to the expansion ROM (see ExpRomAddr and ExpRomData registers). If the expansion ROM is not being accesses, EA0/LEDDPLXN is the Duplex Status LED driver signal.
EWEN	OUTPUT	**Expansion ROM Write Enable.**
EOEN	OUTPUT	**Expansion ROM Output Enable.**

MISCELLANEOUS		
Signal Name	**Signal Type**	**Signal Description**
RSTOUT	OUTPUT	**Reset Output.** RSTOUT is the reset output from the device. The TC9021 will assert RSTOUT when it is being reset. RSTOUT is intended to be used as reset to other circuitry on the adapter.
TEST	INPUT	**Test Mode.** TEST asserted HIGH during reset places the TC9021 in TEST mode. For normal operation, TEST is LOW.
GMII	INPUT	**Physical Layer Mode.**

MISCELLANEOUS		
Signal Name	**Signal Type**	**Signal Description**
		GMII asserted HIGH places the TC9021 in GMII Mode. GMII asserted LOW places the device in TBI Mode.
CLK125	INPUT	**125MHz Clock.** CLK125 is the reference clock used for the TC9021's internal logic.

POWER AND GROUND		
Signal Name	**Signal Type**	**Signal Description**
VCCH	POWER	+3.3 volt power supply for input/output circuits.
GND	GROUND	+3.3 volt return.
VCCL	POWER	+2.5 volt power supply for internal core logic.
GND	GROUND	+2.5 volt return.

6 Acronyms and Glossary

LAN	Local Area Network
MAC	Media Access Control Layer, or a device implementing the functions of this layer (a Media Access Controller)
PCI	Peripheral Component Interface
NIC	Network Interface Cards
FIFO	First In First Out
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
LED	Light Emitting Diode
PHY	Physical Layer, or device implementing functions of the Physical Layer
PCS	Physical Coding Sub-layer
CSMA/CD	Carrier Sense Multiple Access with Collision Detect
FCS	Frame Check Sequence
SFD	Start of Frame Delimiter
CRC	Cyclic Redundancy Check
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
IP	Internet Protocol
VLAN	Virtual LAN
TFD	Transmit Frame Descriptor
RFD	Receive Frame Descriptor
DMA	Direct Memory Access
ACPI	Advanced Configuration and Power Management

7 Standards Compliance

The TC9021 implements functionality compliant with the following standards:

IEEE 802.3 1998 Edition
IEEE 802.3 Full Duplex Flow Control
IEEE 802.3z, 802.3x

IEEE 802.1p, 802.1Q
PCI Local Bus Revision 2.2
PCI Bus Power Management Interface Revision 1.1
ACPI Revision 1.0

8 Functional Description

8.1 PCI Bus Interface

The PCI Bus Interface (PBI) implements the procedures and algorithms needed for the TC9021 to operate in a PCI bus slot as either a PCI bus master or slave. The PBI is also responsible for managing the DMA interfaces and the host processor access to the TC9021 registers. Arbitration logic within the PBI block accepts bus requests from the TxDMA Logic and RxDMA Logic. The PBI also manages interrupt generation for a host processor.

The TC9021 supports all of the PCI memory commands and decides on a burst-by-burst basis which command to use in order to maximize bus efficiency. The list of PCI memory commands is shown below.

Memory Read (MR)
Memory Read Line (MRL)
Memory Read Multiple (MRM)
Memory Write (MW)
Memory Write Invalidate (MWI)

MR is used for all fetches of descriptor information. For reads of transmit frame data, MR, MRL, or MRM is used, depending upon the remaining number of bytes in the fragment, the amount of free space in the TxFIFO, and whether the RxDMA Logic is requesting a bus master operation.

MW is used for all descriptor writes. Writes of receive frame data use either MW or MWI, depending upon the remaining number of bytes in the fragment, the amount of frame data in the RxFIFO, and whether the TxDMA Logic is requesting a bus master operation.

The TC9021 provides a set of registers that control the PCI burst behavior. These registers allow a trade-off to be made between PCI bus efficiency and underrun/overrun frequency.

In support of bus isolation requirements for system states in which the TC9021 is powered down, all TC9021 PCI outputs will enter the tri-state condition when the RSTN is active.

8.2 DMA

The TC9021 implements scatter gather Direct Memory Access (DMA) for moving data from the device to/from the host's system memory. Two independent DMA processes are used to transfer transmit data from host system memory to the TC9021 (transmit DMA), and to transfer receive data from the device to host system memory (receive DMA).

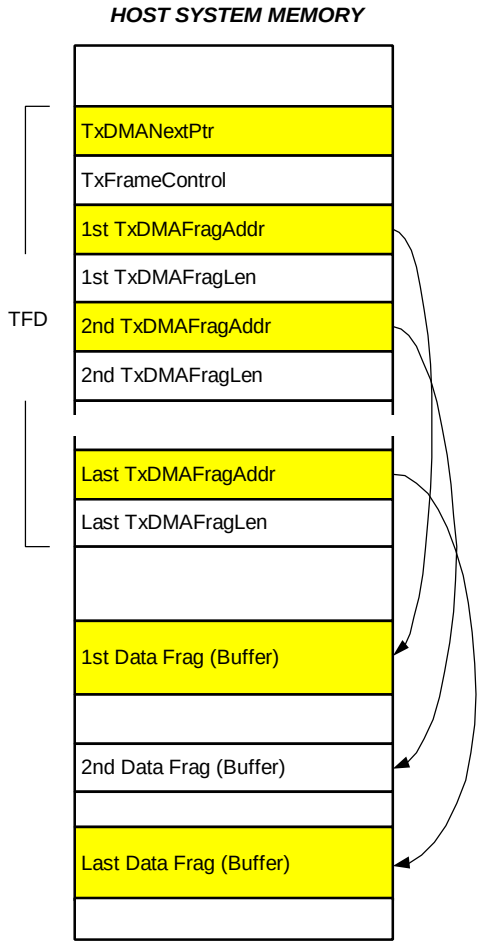
8.2.1 Transmit DMA

To utilize the TC9021 to transmit data onto a Gigabit Ethernet network, the data must be transferred from the host's system memory over the PCI bus.

The locations within system memory which contain the data to be transmitted are indicated to the TC9021 using Transmit Frame Descriptors.

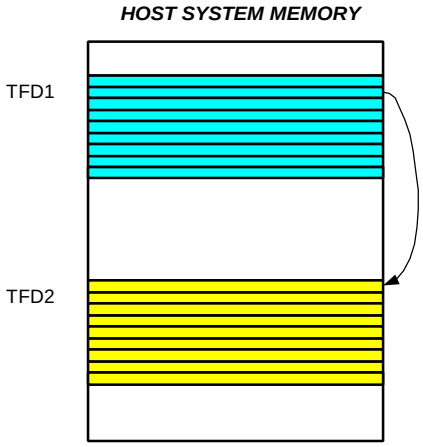
The Transmit Frame Descriptor (TFD) is a data structure containing fields specifying a pointer to another TFD (the TFDNextPtr field), control information (the TFC field), and from one to 15 pointers to locations within system memory containing the Ethernet frame data (the FragInfo fields). The TFD is used to indicate to the TC9021 which blocks of system memory comprise the Ethernet frame data to be transmitted. Each Ethernet frame is described by one and only one TFD.

FIGURE 1: TxDMA Data Structure



The TFD format is covered in the Registers and Data Structures section. TFDs are typically grouped into linked lists (called TFD lists) within system memory by the host system.
The TFDNextPtr field is used to link one TFD to the next in the list. The resulting linked list of TFDs is referred to as the TxDMAList, as shown in Figure 2.

FIGURE 2: TxDMA List of Two TFDs

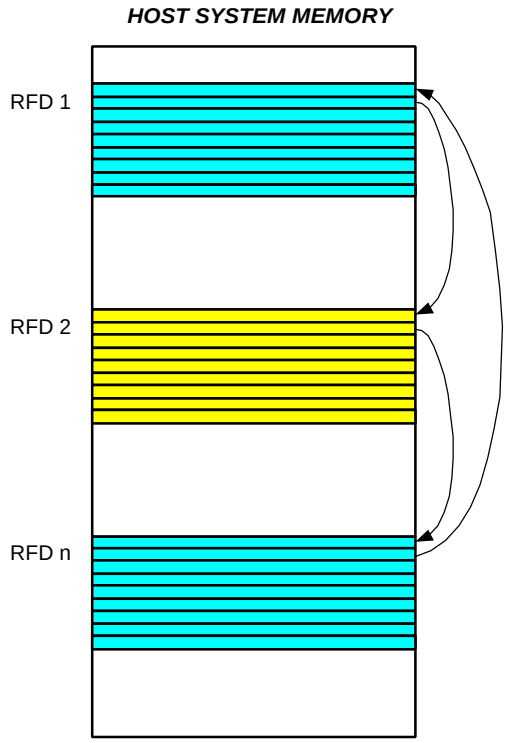


The location of the first TFD in a TFD list is indicated to the device by writing the memory location of the first TFD to the TFDListPtr register.
Upon reset, the TFDListPtr register contains a null value (0x0000000000) indicating to the device that there is no data to transfer via the transmit DMA process. Once a TFD list has been created in system memory, and the location of the first TFD in the list has been written to the TFDListPtr register, the transmit DMA process begins.
There are several cases during transmit DMA operation in which host system interrupts are generated. See section 8.3.1 for details on transmit DMA interrupts.

8.2.1 Receive DMA

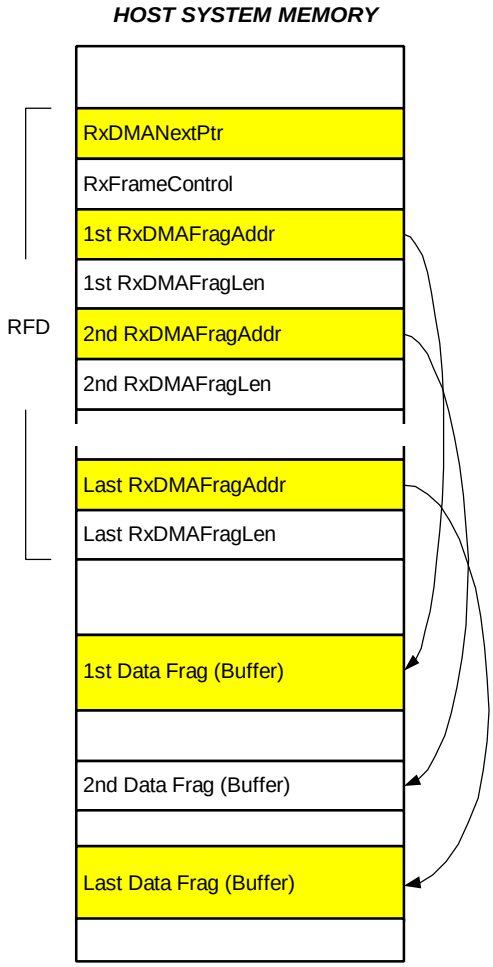
To utilize the TC9021 to receive data from a Gigabit Ethernet network, the received data must be transferred from the device to the host's system memory via the PCI bus by DMA. The locations within system memory reserved for the received data are indicated to device using Receive Frame Descriptors.
The Receive Frame Descriptor (RFD) is a data structure containing fields specifying a pointer to another RFD (the RFDNextPtr field), status information (the RFS field), and one pointer (the Frag-Info field) to a unique, contiguous block of system memory which is reserved for holding the received data. Typically, one RFD will completely specify a single received Ethernet frame. While it is possible to use multiple RFDs to describe a single Ethernet frame, it is not possible to describe multiple Ether-net frames with a single RFD. The RFD format is described in section 8.10.2.
RFDs are typically grouped into linked lists (called RFD lists) within system memory by the host system, as shown below:.

Figure 3: RxDMA List Shown in Ring Configuration



The RFDNextPtr field is used to link RFDs within the list. The location of the first RFD in a RFD list is indicated to the device by writing the memory location of the first RFD to the RFDListPtr register.
Upon reset, the RFDListPtr register contains a value of 0x0000000000 indicating to the device that there is no room in host system memory reserved for received data. The RFD format is covered in the Registers and Data Structures section, while graphically shown below in Figure 4.

Figure 4: RxDMA Data Structure



Once a RFD list has been created in system memory, and the location of the first RFD in the list has been written to the RFDListPtr register, the receive DMA process begins.
There are several cases during receive DMA operation in which host system interrupts are generated. See section 8.3.3 for details on receive DMA interrupts.

8.3 Interrupts

The TC9021generates host system processor interrupts via the PCI bus based on events related to transmit and receive DMA operation. It is the responsibility of the host system to detect these interrupts, identify the corresponding condition which caused the interrupt, and take the appropriate action.
At gigabit per second data rates, interrupts related to Gigabit Ethernet frame transmission and reception can quickly overwhelm a host system processor. The device incorporates several features for minimizing the number of interrupts generated.
These features should be utilized to achieve maximum system performance in Gigabit Ethernet networks.

8.3.1 Transmit DMA Interrupts

Interrupts can be generated by the device based on a number of events related to transmit DMA operation:

TxDMAComplete interrupt is issued after successful transfer of an Ethernet frame to the device via transmit DMA with the TxDMAIndi-cate bit in the TFD's TFC field is a logic 1. Use of this interrupt is not recommended due to the frequency of transmit DMA operations in a Gigabit Ethernet network.

TxComplete interrupt (frame transmission complete without error) is issued after successful transmission of an Ethernet frame which has already been transferred to the device with the TxIndicate bit in the TFD's TFC field is a logic 1. A recommended use of this feature is to avoid setting the TxIndicate bit in every TFD, but instead only set the TxIndicate bit in the last TFD of a TFDList, or in every Nth frame (where N>1).

TxComplete interrupt (frame transmission encountered an error) is issued if an error occurs during transmission of an Ethernet frame which has already been transferred to the device independent of the TxIndicate bit setting in the TFD's TFC field. When an error occurs, the transmit MAC of the device is disabled (and must be re-enabled to resume operation). Transmit DMA operation continues in spite of transmit errors except for the case of a transmit underrun error (indicated by the TxUnderrun bit in the TxStatus register). To resume transmit DMA operation after a transmit underrun error, the transmit DMA, transmit FIFO, and transmit MAC functions within TC9021 must be reset.

IntRequested interrupt is issued after expiration of the TC9021 Countdown timer register. The Countdown timer register can be programmed to generate an interrupt at fixed intervals.

A common use of interrupts during transmit DMA operation is to determine which TFDs have been successfully transmitted so the host system can free the memory occupied by old TFDs. Interrupts however usually incur a significant cost in terms of host system performance, requiring a large percentage of processor time to service. While interrupts are expensive, memory is usually abundant, therefore a trade off which minimizes interrupts in exchange for more memory usage is desirable.

8.3.2 "Interrupt-Less" Transmit DMA

TC9021's transmit DMA can operate without generating host system processor interrupts. In this mode of operation, the host system does not set the TxIndicate or TxDMAIndicate bits in the TFC field of any TFDs used to transfer Ethernet frames from system memory. Thus, an interrupt is not issued by the device to indicate successful DMA transfer or successful transmission of each Ethernet frame. An interrupt will only be issued by the device in the event of a transmit error, but this case should be rare.

Without the use of interrupts, the device provides another mechanism for the host system to determine which Ethernet frames have been successfully transmitted. This mechanism allows the host system to free memory locations holding old TFD lists. This "interrupt-less" mechanism involves using the TxFrameId field of the TxStatus register.

The TxFrameId field of the TxStatus register indicates the last Ethernet frame which was successfully transmitted. Using this information, the host system can infer successful transmission of all Ethernet frames up to the frame indicated by the TxFrameId field of the TxStatus register. Thus, the host system decides when to poll the TxFrameId field of the TxStatus register (for example, when the amount of memory occupied by old TFD lists becomes excessive) and avoid generation of processor intensive interrupts by the device.

8.3.3 Receive DMA Interrupts

Interrupts can be generated by the device based on a number of events related to receive DMA operation:

RxEarly interrupt is issued after receipt of Ethernet frame data from the Gigabit Ethernet network, where the number of bytes received is greater than the value of RxEarlyThresh register. Use of this interrupt is not recommended due to the frequency of Ethernet frame receipts in a Gigabit Ethernet network.

RxDMAComplete interrupt is issued after successful transfer of one or more Ethernet frames (based on the interrupt coalescing configuration) from the device to the host system memory. Interrupt coalescing should be used in conjunction with the RxDMAComplete interrupt given the frequency of frame receipts in a Gigabit Ethernet network.

RxDMAPriority interrupt is issued if a received Ethernet frame contains a Tag Control Information field with priority greater than or equal to the priority set in the RxDMAIntCtrl register.

RFDListEnd interrupt is issued if the end of the RFD list is reached (indicated by an RFDNextPtr field with a value of 0x0000000000), or a RFD with the RFDDone bit of the RFS field with a value of logic 1 is encountered.

8.3.4 Receive DMA Interrupt Coalescing

A common use of interrupts during receive DMA operation is to indicate when new Ethernet frames have been transferred to host system memory.

Interrupts however usually incur a significant cost in terms of host system performance, requiring a large percentage of processor time to service. One way to improve the performance of the host system is to optimize the number of interrupts issued by the device related to receive DMA operation.

Depending upon the arrival rate of Ethernet frames and user programmable parameters, a single interrupt can be used to indicate multiple Ethernet frames have been received. The host will be able to handle multiple received frames within the same interrupt service routine.

While minimizing interrupts can improve host system performance, it can also require more host system memory usage, and increase network latency. Therefore, a balance between interrupt frequency and network latency must be reached to optimize performance.

8.4 ACPI

The TC9021 supports operating system directed power management according to the ACPI specification.
Power management registers in the PCI configuration space, as defined by the PCI Bus
Power Management Interface specification, Revision 1.0 are described in section 8.10.

8.4.1 Power Management States

The TC9021 supports several power management states. The PowerState field in the PowerMgmtCtrl register determines TC9021's current power state.

The power states are defined as follows:

D0 Uninitialized (power state 0, D0u) is entered as a result of hardware reset, or after a transition from D3 Hot to D0. This state is the same as D0 Active except that the PCI configuration registers are uninitialized. In this state, the device is unable to respond to PCI I/O or memory cycles and can not operate as a PCI master; it responds to PCI configuration cycles only. The device cannot signal wake events (WAKE/PMEN) from the D0u state.

D0 Active (power state 0) is the normal operational power state for the device. In this state, the PCI configuration registers have been initialized by the system, including the IoSpace, MemorySpace, and BusMaster bits in the Config Command register, so the device is able to respond to PCI I/O, memory and configuration cycles and can operate as a PCI master. In Forced Configuration mode or WakeOnLan mode (set by the WakeOnLanEnable bit in the WakeEvent register), TC9021 bypasses the D0u state and will enter the D0a state after power up or hardware reset. The device cannot signal wake events (WAKE/PMEN) from the D0a state.

D1 (power state 1) is a "light-sleep" state. The device optionally supports this state determined by the D1Support bit in the ConfigParm word in the EEPROM. The D1 state allows transition back to D0 with no delay. In this state, the device responds to PCI configuration accesses, to allow the system to change the power state. In D1 the device does not respond to any PCI I/O or memory accesses. The TC9021's function in the D1 state, if power management events are enabled (PmeEn bit set), is to recognize wake events and pass them on to the system by asserting the PMEN signal on the PCI bus.

D2 (power state 2) is a partial power-down state. The device optionally supports this state determined by the D2Support bit in the ConfigParm word in the EEPROM. D2 allows a faster transition back to D0 than is possible from the D3 state. In this state, the device responds to PCI configuration accesses, to allow the system to change the power state. In D2 the device does not respond to any PCI I/O or memory accesses. The TC9021's function in the D2 state, if power management events are enabled (PmeEn bit set), is to recognize wake events and pass them on to the system by asserting the PMEN signal on the PCI bus.

D3 Hot (power state 3, D3h) is the power down state for the device if power management events are disabled (via PmeEn bit in the PowerMgmtCtrl register). In D3 Hot, the device loses all PCI configuration information except. for the value in PowerState. In this state, the device responds to PCI configuration accesses, to allow the system to change the power state back to D0 Uninitialized. In D3 Hot, the device does not respond to any PCI I/O or memory accesses. The TC9021's main responsibility in the D3 Hot state, if power management events are enabled

(PmeEn bit set), is to recognize wake events and signal those to the system by asserting the PMEN signal on the PCI bus.
D3 Cold (power state 3, D3c) is the power down state for the device if power management events are disabled (via PmeEn bit in the PowerMgmtCtrl register). When power is restored, the system guarantees the assertion of hardware reset, which puts the device into the D0 Uninitialized state. The TC9021's main responsibility in the D3 Cold state, if power management events are enabled (PmeEn bit set), is to recognize wake events and signal those to the system by asserting the PMEN signal on the PCI bus. Since the PCI bus power is removed during D3 Cold state, the device requires auxiliary power supply to support power management event detection.

8.5 Wake On LAN

Wake on LAN is a key component of the IBM/Intel® Advanced Manageability Alliance (AMA) initiative.
The TC9021 implements a portion of the Wake On LAN functionality defined by the AMA initiative. Specifically, the device can be configured to respond to wake up frames sent by a Wake On LAN management station.

8.5.1 Power Management Events

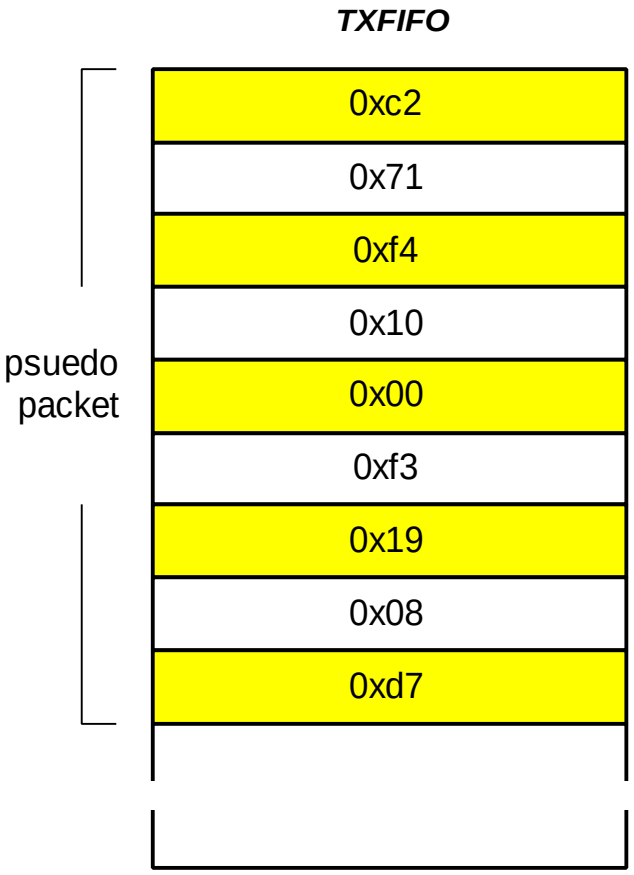
The TC9021 can generate power management events, sometimes also called wake events, to the host system as a result of Wake Packet reception, Magic Packet reception, or due to a change in the link status. The WakeEvent register gives the host system control over which of these events are passed to the system. Wake events are signaled over the PCI bus using the PMEN signal.
A wake event can only be recognized if the device is in one of the D1, D2, or D3 power states. When the device is in either of the two D0 power states, it will not be able to signal wake events.
When a desired wake event occurs, the device sets the appropriate event bit in the WakeEvent register, sets the PmeStatus bit in the PowerMgmtCtrl register, and asserts the WAKE/PMEN pin.
The host system responds to PMEN by scanning the power management configuration registers of all devices, finding the PmeStatus set in TC9021's PowerMgmtCtrl register. The operating system then clears the PmeEn bit in the PowerMgmtCtrl register causing WAKE/PMEN to be de-asserted.

8.5.1.1 Wake Packet

A Wake Packet event is controlled by the WakePktEnable bit in WakeEvent register. The WakePktEnable bit has no effect when TC9021 is in the D0 power state, as the wake process can only take place in states D1, D2, or D3. When the device detects a Wake Packet, it signals a wake event on WAKE (if WAKE assertion is enabled), and sets the WakePktEvent bit in the WakeEvent register. The device can signal that a wake event has occurred when it receives a pre-defined frame from another station. The host system transfers a set of frame data patterns into the transmit FIFO using the TxDMA function before placing the device in a power-down state. Once powered down, the device compares receive frames with the frame patterns in the transmit FIFO. When a matching frame is received (and also passes the filtering mode set in the ReceiveMode register), a wake event is signaled.
Frame patterns are written to the transmit FIFO in a single "pseudo-packet". Prior to transferring this pseudo-packet, the host system should first set the TxReset in the AsicCtrl (to reset the transmit FIFO pointers and prevent transmission) then prepare a TFD that points to a single data buffer. The buffer should contain one or more frame patterns placed contiguously. The number of frame patterns is limited by the transmit FIFO size. The FragLen field in the TFD must exactly equal the sum of the frame pattern bytes. Also, the host system must set the WordAlign field to 'x1' in the TFC field of the TFD to prevent frame word-alignment. Finally, the host system must write the TFD's address to the TFDListPtr register to transfer the frame into the transmit FIFO.
The frame patterns in the transmit FIFO specify which bytes in the incoming frames are to be examined. A CRC is calculated over these bytes and compared with a CRC value supplied in the frame pattern. This matching technique may result in false wake events being reported to the host system. Each wake packet pattern contains one or more byte-offset/byte-count pairs, an end-of-pattern symbol, and a 4-byte CRC value. The byte-offset indicates the number of frame bytes to be skipped in order to reach the next group of bytes to be included in the CRC calculation. The byte-count. indicates the number of bytes in the

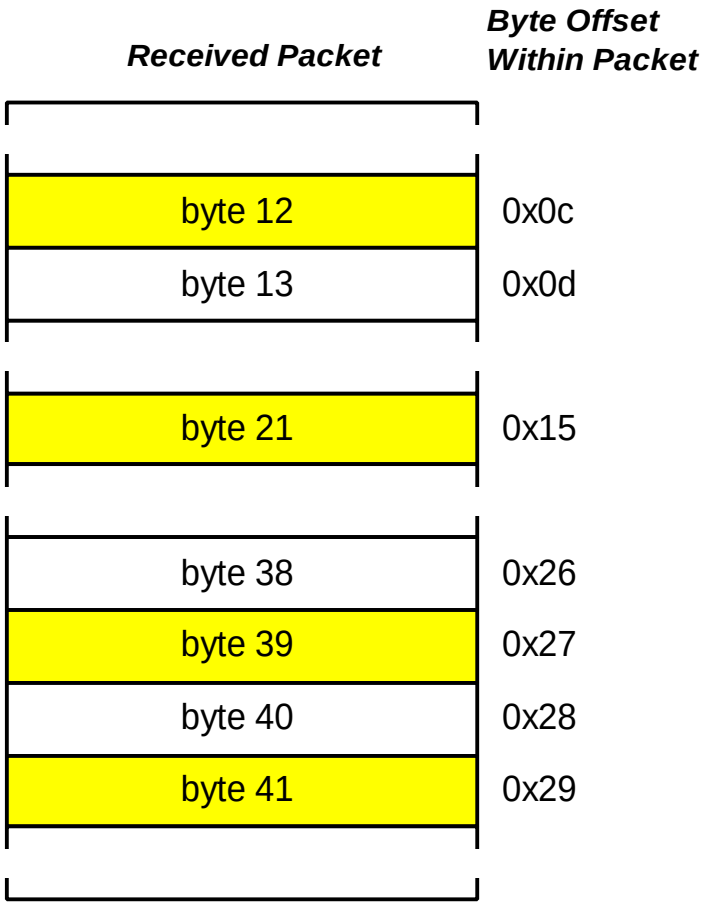
next group to be included in the CRC calculation. End-of pattern, which is a byte value of 0x00, indicates the end of the pattern for that wake frame. Immediately following the end-of-pattern is a 4-byte CRC. The CRC calculation uses the same polynomial as the Ethernet MAC FCS. The pseudo packet frame patterns are described in section 8.10.
An example pseudo-packet (based on the ARP packet example from Appendix A of the "OnNow Network Device Class Power Management Specification") loaded into the transmit FIFO of the TC9021 is shown in Figure 5.

FIGURE 5: Example Psuedo Packet



Using the pseudo packet in Figure 5, the device will assert a wake event if a packet of the form shown in Figure 6 is received whereby a 32-bit CRC over the indicated bytes of the received packet yields the value 0xF31908D7.

FIGURE 6: Example Wake Packet

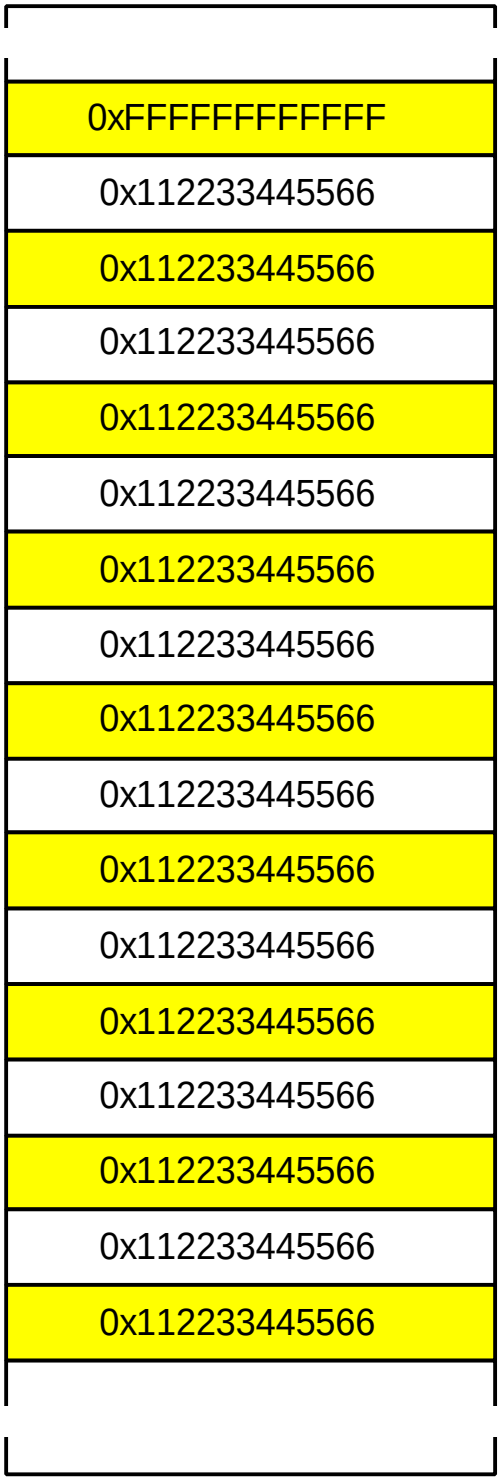


8.5.1.1 Magic Packet

The TC9021 also supports Magic Packet™ technology developed by Advanced Micro Devices to allow remote wake-up of a sleeping station on a network via transmission of a special frame. Once the device has been placed in Magic Packet mode and put to sleep, it scans all incoming frames addressed to it for a data sequence consisting of 16 consecutive repetitions of its own 48-bit Ethernet MAC StationAddress. This sequence can be located anywhere within the frame, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of 0xFF. For example, if the MAC address programmed into the StationAddress register is 0x11:22:33:44:55:66, then the device would be scanning for the frame data shown in Figure 7.

FIGURE 7: Example Magic Packet

Received Packet



Magic Packet wake up is controlled by the MagicPktEnable bit in the WakeEvent register. A wake event can only take place in the D1, D2, or D3 states, and the MagicPktEnable bit has no effect when the device is in the D0 power state. The Magic Packet must also pass the address matching criteria set in ReceiveMode register. A Magic Packet may also be a broadcast frame. When the device detects a Magic Packet, it signals a wake event on

WAKE (if WAKE assertion is enabled), and sets the MagicPktEvent bit in the WakeEvent register.

8.5.1.1 Link Status Change

The TC9021 can also signal a wake event when it senses a change in the network link state, either from LINK_OK to LINK_FAIL, or vice versa. Link state wake is controlled by the LinkEventEnable bit in the WakeEvent register. At the time LinkEventEnable is set by the host system, the device samples the current link state. It then waits for the link state to change. If the link state changes before the device returns to state D0 or LinkEventEnable is cleared, LinkEvent is set in WakeEvent, and (if it is enabled) the WAKE/PMEN signal is asserted.

8.6 FIFO

The TC9021 incorporates on chip transmit and receive FIFOs. The transmit FIFO is 16kbytes (16,384 bytes) in length while the receive FIFO is 32kbytes (32,768 bytes) in length.

8.7 MAC

The MAC block implements the IEEE Ethernet 802.3 Media Access Control functions with Full Duplex and Flow Control enhancements. In half duplex mode, the MAC implements the Carrier Sense Multiple Access with Collision Detect (CSMA/CD) protocol. Full duplex mode by definition does not utilize CSMA/CD, allowing data to be transmitted on demand. An optional flow control mechanism in full duplex mode is provided via the MAC Control PAUSE function. Additionally, the MAC also performs these functions in either half or full duplex mode:

Optional transmit frame check sequence (FCS) generation
Padding to the minimum legal frame size
Preamble and SFD generation
Preamble and SFD removal
Receive frame FCS checking and optional FCS stripping
Receive frame destination address matching
Support for multicast and broadcast frame reception or rejection (via filtering) In addition, the MAC is responsible for generation of hardware signals to update the internal statistics counters.

8.7.1 VLAN

Virtual Local Area Network (VLAN) technology is used to regulate broadcast and multicast traffic in switched Ethernet networks. VLAN technology utilizes Ethernet frame tagging, providing Ethernet switches a mechanism to correlate a specific Ethernet frame with a specific group of end stations.
Using this correlation, Ethernet switches in a network are able to regulate broadcast and multi-cast VLAN tagged frames, forwarding such frames only to those nodes which are members of the same VLAN (instead of to all nodes). In this way, broadcast and multicast network utilization is mini-mized.
The IEEE defines VLANs as follows:

VLANs facilitate easy administration of logical groups of stations that can communicate as if they were on the same LAN. They also facilitate easier administration of moves, adds and changes in members of these groups.
Traffic between VLANs is restricted. Bridges forward unicast, multicast and broadcast traffic only on LAN segments that serve the VLAN to which the traffic belongs.
As far as possible, VLANs maintain compatibility with existing bridges and end-stations.

Detailed information on VLAN implementation is located in the following standards:

IEEE 802.1p Traffic Class Expediting and Dynamic Multicast Filtering (now part of ISO/IEC 15802-3: 1998). Introduces the concept of priority processing in Ethernet bridges and specifies the registration protocols used to disseminate switching rules between nodes and switches in a network. Also defines GMRP and GARP.
IEEE 802.1Q Virtual Bridged Local Area Networks (also now part of ISO/IEC 15802-3:1998). Specifies the operation of VLAN enabled Ethernet bridges, and defines the tagged frame format.

IEEE 802.3ac Frame Extensions for Virtual Bridged Local Area Networks (VLAN) Tagging on 802.3 Networks. Modifies the IEEE 802.3 specification to accommodate tagging for VLANs as specified in IEEE 802.1Q.

The TC9021 supports VLANs with the following functions:

Transmission and reception of VLAN tagged frames, increasing the maximum frame size by four octets.

VLAN tags for transmit frames may be applied either by the host system prior to transfer of the frame to the device via the transmit DMA process, or by the device via the VLAN tag information specified in the TFC or the VLANTag register. The TFC VLANTagInsert field, and MACCtrl register AutoVLANtagging bit determines the source for VLAN frame tagging with the TFC VLANTagInsert having priority over the MACCtrl register AutoVLANtagging bit.

Any VLAN tagged frames received by the device may be transferred to the host system unmodified, or stripped of all VLAN tags as determined by the MACCtrl register AutoVLANtagging bit. For any received frame which contains a VLAN tag, regardless of the state of the MACCtrl register AutoVLANuntagging bit, the VLAN tag is copied to the RFS TCI field.

The priority of VLAN tagged frames received by the device is detected. Based on a programmable received frame priority level, an interrupt is asserted.

8.7.2 Layer 3/4 Checksums

The Ethernet Carrier Sense Multiple Access with Collision Detect (CSMA/CD) protocol comprises a portion of Layer 2 within the Open Systems Inter-connect (OSI) Seven Layer Model of network systems.

Ethernet incorporates a CRC capability (via the FCS field) in an attempt to check for errors during transmission. Higher layer protocols which utilize Ethernet may also utilize checksums in addition to the Ethernet FCS. These higher layer protocol checksum are typically calculated by the host system, and inserted within the Ethernet frame (for transmit data) prior to frame transfer to the device via the transmit DMA process. Similarly, higher layer protocol checksums within received Ethernet frames are verified by the host system after the frames have been transferred from the device via receive DMA process.

The TC9021 can perform checksum calculations, and verifications for three popular higher layer protocols.

Internet Protocol version 4 (Layer 3 within the OSI model) defined in RFC 791
Transmission Control Protocol (Layer 4 within the OSI model) defined in RFC 793
User Datagram Protocol (Layer 4 within the OSI model) defined in RFC 768

By configuring the TC9021 to perform the check-sum calculations for the supported protocols, the host system work load is lightened resulting in higher performance. It is the host system's responsibility to assure that the respective checksum functions are only enabled for Ethernet frames which contain the respective layer 3/4 data. That is, if an Ethernet frame does not contain an IP datagram, the IPChecksumEnable bit within the TFC field of the frame's TFD must be a logic 0.

Utilization of the device layer 3/4 checksum verification capability for receive data does not require any register configuration. The checksum verification capabilities are always active. The host system decides on a frame by frame basis how to utilize the layer 3/4 checksum verification functions.

For the last RFD of a received Ethernet frame, the RFS field IPDetected, TCPDetected, and UDPDetected bits will be a logic 1 to indicate if the received frame contains an IP datagram, TCP segment, and/or UDP segment.

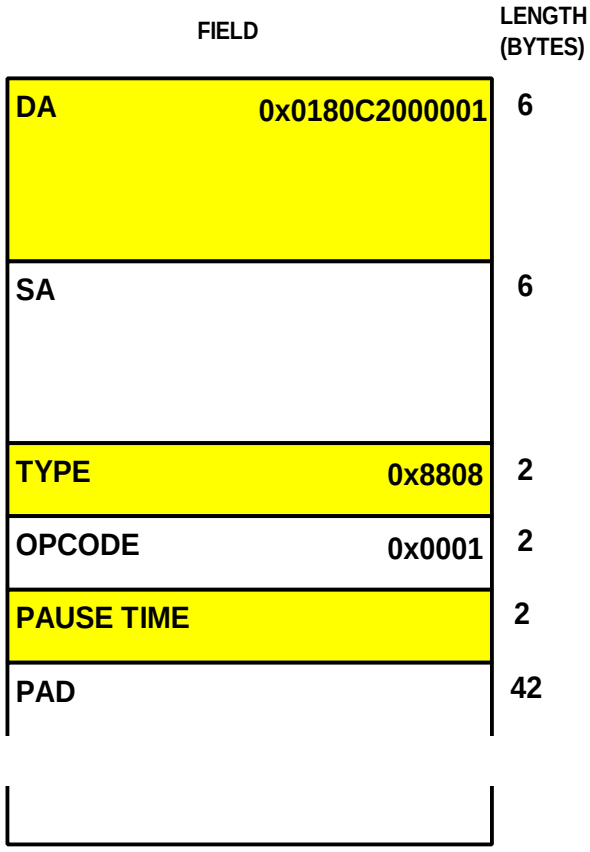
If any of the IPDetected, TCPDetected, and/or UDP-Detected bits within the RFS field of the received frame is a logic 1, then the host system may examine the IPError, TCPError, and UDPError bits within the RFS field to verify the respective layer 3/4 checksums for the received frame. Separate host system algorithms to verify the checksums are not necessary, but may still be performed.

The IPCheckSumErrors, TCPCheckSumErrors, and UDPCheckSumErrors statistic registers will count the number of received frame's which contain an IP datagram, TCP segment, and/or UDP segment where the respective layer 3/4 checksum calculation within the device failed.

8.7.3 Flow Control

The IEEE 802.3x Full Duplex standard defines a special frame known as the PAUSE MAC Control frame. The PAUSE frame is used to implement flow control in full duplex networks allowing stations on opposite ends of a full duplex link the ability to inhibit transmission of data frames for a specified period of time. The PAUSE frame format is defined as shown in Figure 8.

FIGURE 8: PAUSE Frame.



The TC9021 supports both asymmetric and symmetric IEEE 802.3 flow control via the MAC Control PAUSE function. Any IEEE 802.3 flow control compliant node receiving a PAUSE control frame must inhibit frame transmission for the amount of time specified in the PAUSE control frame. The pause time is specified in pause quanta (in Gigabit Ethernet, a pause quanta is 512 bit times and a bit time is 1ns). The maximum pause time is 65,535 pause quanta, or 33.6ms.

Asymmetric operation corresponds to the device acting on PAUSE frames received from the network.

Symmetric operation corresponds to the device both acting on received PAUSE frames, and transmitting PAUSE frames onto the network.

Use of asymmetric and symmetric flow control is typically determined during auto negotiation (see section 8.9.1).

When participating in symmetric flow control operation, transmit PAUSE frames can be generated by the host system, or automatically by the device.

The host system may use any mechanism to determine when to use DMA to transfer a PAUSE frame to the device. Automatic generation of PAUSE control frames by the device is related to the state of the receive FIFO. If the receive FIFO fills beyond a host system configurable point (the flow control on threshold, as defined by the FlowOnThresh register), the device will automatically transmit a PAUSE frame in an attempt to halt the transmitting node. The flow control on threshold must be chosen carefully to account for receiving frames already in transit. A general rule is to set the flow control on threshold offset (the difference between the maximum size of the FIFO, and the flow

control on threshold) equal to or greater than twice the size (in bytes) of the maximum expected receive frame size.
For the TC9021 automatic flow control mechanism to function properly, the receive FIFO must empty beyond a second configurable point (the flow control off threshold, as defined by the FlowOffThresh register) within 33.6ms (the amount of time the opposite node will remain paused when receiving the TC9021 generated PAUSE frame). When the TC9021 receive FIFO empties beyond the flow control off threshold, a second PAUSE frame (with pause time equal to zero) is transmitted to indicate the device is ready to receive more data. If the device receive FIFO flow control off threshold is not crossed within 33.6ms after the maximum time PAUSE frame is transmitted, the TC9021 receive FIFO will likely overrun. This condition indicates a problem with the host system, in that data is not being transferred from the TC9021 receive FIFO at a sufficient rate to keep up with the Gigabit Ethernet LAN segment over an extended period of time.
The flow control thresholds must be chosen carefully to account for the time required by the host system to empty the receive FIFO.
Receive flow control operation of the device is controlled via the MACCtrl register RxFlowControlEnable bit. Transmit flow control operation of the device (automatic PAUSE frame generation) is controlled via the MACCtrl register TxFlowControlEnable bit and the FlowOnThresh and FlowOffThresh registers.

8.8 GMII

The TC9021 can support a variety of physical signaling schemes via the IEEE 802.3 defined Gigabit Media Independent Interface (GMII). Through the GMII, the device supports various physical layer implementations of the Gigabit Ethernet standard. The GMII provides a general-purpose interface between an 802.3 MAC and various physical layer devices, and is comprised of two independent components. The data interface provides separate, 8-bit wide paths for receive and transmit data, as well as independent clock and control signals. The management interface is a bidirectional, serial link that provides the device access to registers residing within the physical layer device. The host system controls the GMII management interface through the PhyCtrl register.
Since the GMII is independent of the signaling method (1000BASE-X, 1000BASE-T), it is possible to use it to support numerous Ethernet LAN types depending upon the availability of GMII-compliant PHY devices.
It is most likely that a physical layer device connected to TC9021's GMII will include implementation of the 802.3 Auto-Negotiation function. For instance, a PHY device may be able to auto-negotiate various parameters of Gigabit Ethernet operation. A host system attempting to determine link status should check the Auto-Negotiation function contained in the GMII-based PHY device through the GMII management interface of the TC9021.

8.9 PCS

The TC9021 implements an IEEE 802.3 compliant Physical Coding Sublayer (PCS) for use with PHY devices using the TBI. The TC9021 PCS implements the following functions:

8B10B Encoder and Decoder
Transmit State Machines
Auto-negotiation State Machine
Receive State Machine
Synchronization State Machine
Management Registers

8.9.1 Auto-Negotiation

The TC9021 PCS layer implements IEEE 802.3 1000BASE-X auto-negotiation for Gigabit Ethernet.
The auto-negotiation function is controlled via the PCS registers internal to the TC9021 PCS layer implementation. The host system must utilize these registers in order to properly configure the TC9021 for compatible operation with the TC9021's link partner. The host system responsibilities are as follows:

Enable or disable the device for auto-negotiation via the Auto-Negotiation Enable bit of the PCS Control register.
Configure the PCS Advertisement register to indicate the capabilities of the Gigabit Ethernet implementation.

If there is any Next Page data to send, and/or if the host system is willing to accept Next Page data, configure the Next Page bit of the Advertisement register.
Re-start auto-negotiation using the Control register.
Read the Page Received bit of the Expansion register to determine when the link partner's base page data has been received. This is only necessary if Next Page transmissions are to follow. If there are to be no Next Page transmissions, the Control register Auto-Negotiation Complete bit can be used to determine when to read the link partner's base page data.
Read the LinkPartnerBasePage register to determine the link partner's capabilities.
If the LinkPartnerBasePage register Next Page bit is 1 (indicating the link partner is able to accept and/or would like to transmit Next Page information) transmit the first page of the Next Page information to the link partner via a write to the NextPage register. If there is no Next Page data to transfer, write 0x2001 to the Nex-tPage register.
After writing to the NextPage register, read the Expansion register, Page Received bit to determine when new Next Page data from the link partner has arrived.
When new Next Page data has arrived from the link partner, read the LinkPartnerNextPage register.
For multiple Next Page data transfers, the host system must repeat the process of writing to the NextPage register, reading the Expansion register, and reading the LinkPartnerNextPage register until a logic 0 is read in the LinkPartnerNextPage register Next Page bit is read or a value of 0x2001 for the Next Page data is read and there are no more Next Page transfers required.
Optionally, the NextPage register Acknowledge 2 bit may be used to indicate to the link partner that received Next Page data will be acted upon. A logic 1 in the Acknowledge 2 bit of the LinkPartnerNextPage register indicates the link partner is able to perform the task defined in the Next Page message.
The host system must implement the Priority Resolution function (specified in IEEE 802.3 1998 Edition Clause 37.2.4.2) to resolve the mode of operation for the device. Priority Resolution applies to the duplex, and pause modes of operation. The rules for resolution are contained in the IEEE standard, and duplicated here for reference.

Table 3: Duplex Mode Priority Resolution

Local Device Advertised Duplex Mode	Link Partner Advertised Duplex Mode	Local Device Duplex Mode Resolution
Half	Half	Half
Half	Full	Half
Full	Half	Half
Full	Full	Full

Table 4: PAUSE Mode Priority Resolution

Local Device Advertised Pause Mode		Link Partner Advertised Pause Mode		Local Device Pause Mode Resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR	
0	0	-	-	Disable PAUSE Transmit and Receive
0	1	0	-	Disable PAUSE Transmit and Receive
0	1	1	0	Disable PAUSE Transmit and Receive
0	1	1	1	Enable PAUSE Transmit, Disable PAUSE Receive
1	0	0	-	Disable PAUSE Transmit and Receive
1	0	1	-	Enable PAUSE Transmit and Receive

Local Device Advertised Pause Mode		Link Partner Advertised Pause Mode		Local Device Pause Mode Resolution
PAUSE	ASM_DIR	PAUSE	ASM_DIR	
1	1	0	0	Disable PAUSE Transmit and Receive
1	1	0	1	Enable PAUSE Receive, Disable PAUSE Transmit
1	1	1	-	Enable PAUSE Transmit and Receive

After resolving the modes of operation, the host system must configure the TC9021 MAC-Ctrl register DuplexSelect bit, RxFlowControlEnable bit (to configure PAUSE MAC Control Frame receive functionality), and the Duplex Mode bit of the PCS Control register (used only for properly setting the EA0/LEDDPLXN LED signal). PAUSE Mac Control Frame transmit functionality is controlled entirely by the host system.
Finally, the host system must configure functionality negotiated via the Next Page data transfers.

8.10 Registers and Data Structures

The TC9021 utilizes both on chip registers, as well as data structures located within the host system memory, and external non-volatile memory devices.

8.10.1 Transmit DMA Data Structure

The host system uses the Transmit Frame Descriptor (TFD) to transfer data from host system memory to TC9021 via the transmit DMA process. TFDs must be located within host system memory on quad word (64 bit) boundaries. The TFD format is shown in Table 5.

TABLE 5: TC9021 TFD Format

64 BITS	ADDR OFFSET
TFDNextPtr	0x00
TFC	0x08
Fraglnfo0	0x10
Fraglnfo1	0x18
Fraglnfo2	0x20
Fraglnfo3	0x28
Fraglnfo4	0x30
Fraglnfo5	0x38
Fraglnfo6	0x40
Fraglnfo7	0x48
Fraglnfo8	0x50
Fraglnfo9	0x58
Fraglnfo10	0x60
Fraglnfo11	0x68
Fraglnfo12	0x70
Fraglnfo13	0x78
Fraglnfo14	0x80

8.10.1.1 TFDNextPtr

Class..... Transmit DMA Data Structure
Base Address ..... TFD starting address in system memory
Address Offset 0x00

Width ..... 64 bits
Transmit Frame Descriptor Next Pointer field.

Bit	Bit Name	Bit Description
39..0	TFDNextPtr	TFD Next Pointer indicates the location in system memory of the next TFD. Only the lower 40 bits of the TFDNextPtr field are valid, the upper 24 bits are reserved. A value of 0x0000000000 in this field indicates there are no more TFDs ready for transfer.
63..40	Reserved	Reserved for future use. Write as zero, ignore on read.

8.10.1.2 TFC

Class..... Transmit DMA Data Structure
Base Address ..... TFD starting address in system memory
Address Offset 0x08
Width ..... 64 bits
Transmit Frame Control field.

Bit	Bit Name	Bit Description
15..0	FrameId	Frame Identification associates the data referenced by this TFD to a specific Ethernet frame.
17..16	WordAlign	Word Alignment bits determine the boundary to which transmit frame lengths are rounded up in the transmit FIFO, and transmitted onto the network medium. **Bit 17** **Bit 16** **Alignment** 0 0 Align to Double Word 1 0 Align to Word X 1 Alignment Disabled
18	TCPChecksumEnable	Transmission Control Protocol Checksum Enable indicates the host system, or the device will calculate and insert the TCP checksum as defined in RFC 793. A logic 1 indicates the device should calculate the TCP checksum. TCPChecksumEnable should only be set if the Ethernet frame referenced by this TFD contains TCP data. For TFD's which do not contain TCP data, TCPChecksumEnable MUST be 0. In addition, if TCPChecksumEnable is set, FCSAppendDisable MUST be 0. The device must calculate and append the FCS when performing TCP checksum calculation and insertion.
19	UDPChecksumEnable	User Datagram Protocol Checksum Enable indicates the host system, or the device will calculate and insert the UDP checksum as defined in RFC 768. A logic 1 indicates the device should calculate the UDP checksum. UDPChecksumEnable should only be set if the Ethernet frame referenced by this TFD contains UDP data. For TFD's which do not contain UDP data, UDPChecksumEnable MUST be 0. In addition, if UDPChecksumEnable is set, FCSAppendDisable MUST be 0. The device must calcuate and append

Bit	Bit Name	Bit Description
		the FCS when performing UDP checksum calculation and insertion.
20	IPChecksumEnable	Internet Protocol Checksum Enable indicates the host system, or the device will calculate and insert the IP checksum as defined in RFC 791. A logic 1 indicates the device should calculate the IP checksum. IPChecksumEnable should only be set if the Ethernet frame referenced by this TFD contains IP data. For TFD's which do not contain IP data, IPChecksumEnable MUST be 0. In addition, if IPChecksumEnable IS SET, FCSAppendDisable MUST be 0. The device must calculate and append the FCS when performing IP checksum calculation and insertion.
21	FCSAppendDisable	Frame Check Sequence Append Disable is set by the host system to prevent the device from appending the 4-byte Frame Check Sequence(FCS) to the end of the current frame. In this case the host system must supply the frame's FCS as part of the data transferred by the transmit DMA. An exception exists when a transmit underrun occurs. In this case a guaranteed invalid FCS will be appended to the frame by the device. When FCSAppendDiasable is cleared, the device will compute and append the FCS to the transmit frame referenced by this TFD. When using TCPChecksumEnable, UDPChecksumEnable, and/or IPChecksumEnable, the FCSAppendDisable bit MUST be set to logic 0 and the host system MUST NOT append an FCS to the Ethernet frame.
22	TxIndicate	Transmit Indicate is set by the host system to request a TxComplete interrupt upon completion of frame transmission by the MAC. If TxIndicate is cleared, no interrupt of transmission completion will be issued by the device, unless a transmit error occurs.
23	TxDMAIndicate	Transmit DMA Indicate is set if the host system desires a TxDMAComplete interrupt upon completion of the transmit DMA process for this frame.
27..24	FragCount	Fragment Count indicates the number of fragments (from 1 to 15 fragments) used by this TFD. A value of 0 indicates this TFD contains no data to be transferred to the devicey.
28	VLANTagInsert	VLAN Tag Insert indicates that the VLAN information specified in VID, CFI, and UserPriority fields, the Length/Type field of the Ethernet frame specified by this TFD will be set to the value 0x8100 to indicate the frame is VLAN tagged.
30..29	Reserved	Reserved for future use. Write as zero, ignore on read.
31	TFDDone	Transmit Frame Descriptor Done is used as an ownership bit to indicate whether the host system, or the device "owns" (or is currently processing and/or modifying) the TFD. The device will not transfer the TFD from host system memory until a logic 0 is written to the TFDDone bit by the host system. The device will write a logic 1 to the TFDDone bit upon completion of the transmit DMA process for this TFD.
43..32	VID	VLAN Identifier specifies the VID portion of the Tag Control Information (TCI) field within an Ethernet frame VLAN tag(see section 8.7.1). The VID is only valid if the VLANTagInsert bit is a logic 1.
44	CFI	Canonical Format Indicator specifies the CFI portion of the Tag Control Information (TCI) field within an Ethernet frame VLAN tag(see section 8.7.1). The CFI is only valid if the VLANTagInsert bit is a logic 1.
47..45	UserPriority	User Priority specifies the UserPriority portion of the Tag Control Information (TCI) field within an Ethernet frame VLAN tag (see section 8.7.1). The UserPriority is only valid if the VLANTagInsert bit is a logic 1.
63..48	Reserved	Reserved for future use. Write as zero, ignore on read.

8.10.1.3 FragInfo

Class..... Transmit DMA Data Structure

Base Address ..... TFD starting address in system memory
Address Offset ..... 0x10 + n * 0x8 (n = fragment number = 0x0, 0x1, 0x2... 0xE)
Width ..... 64 bits
Fragment Information fields (up 15 in a single TFD) indicate a block of contiguous system memory containing a portion of the frame data to be transmitted. The fragments may be located anywhere in system memory, and need not be contiguous.

Bit	Bit Name	Bit Description
39..0	FragAddr	Fragment Address indicates the location within host system memory of the first byte of the data fragment. Fragments can be located anywhere within a 40 bit (1,099,511,627,776 or 1 Terabyte) memory space.
47..40	Reserved	Reserved for future use. Write as zero, ignore on read.
63..48	FragLen	Fragment Length indicates the length of the fragment in bytes. Fragments can range from zero to 64k (65,536) bytes in length.

8.10.2 Receive DMA Data Structure

The host system uses the Receive Frame Descriptor (RFD) to transfer data from the device to host system memory via the receive DMA process. RFDs must be located within host system memory on quad word (64 bit) boundaries. The RFD format is shown in Tabl e 6.

TABLE 6: TC9021 RFD Format

64 BITS	ADDR OFFSET
RFDNextPtr	0x00
RFS	0x08
FragInfo0	0x10

8.10.2.1 RFDNextPtr

Class..... Receive DMA Data Structure
Base Address ..... RFD starting address in system memory
Address Offset 0x00
Width ..... 64 bits
Receive Frame Descriptor Next Pointer field.

Bit	Bit Name	Bit Description
39..0	RFDNextPtr	RFD Next Pointer indicates the location in system memory of the next RFD. A value of 0x0000000000 in this field indicates there are no more RFDs ready for data.
63..48	Reserved	Reserved for future use. Write as zero, ignore on read.

8.10.2.2 RFS

Class..... Receive DMA Data Structure
Base Address ..... RFD starting address in system memory
Address Offset 0x08
Access Mode ..... Read/Write
Width ..... 64 bits
Receive Frame Status field.

Bit	Bit Name	Bit Description
15..0	RxFrameLen	Receive Frame Length indicates the length in bytes of the received Ethernet frame. If the RFD, FragInfo field's FragLen field is less than the Ethernet frame length, multiple RFDs are required to store the frame. In this case, the RxFrameLen field of the RFS in the last RFD will indicate the actual

Bit	Bit Name	Bit Description
		Ethernet frame length, while all other RxFrameLen fields in the series of RFDs used to store the frame will be 0x0000.
16	RxFIFOOverrun	Receive FIFO Over Run indicates the received frame incurred a FIFO over run error. RxFIFOOverrun is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
17	RxRuntFrame	Receive Runt Frame indicates the received frame was a runt (a frame which is less than 60 octets in length, measured from the DA field to the end of the Data field). RxRuntFrame is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
18	RxAlignmentError	Receive Alignment Error indicates the received frame incurred an alignment error (alignment errors are not encountered in Gigabit Ethernet). RxAlignmentError is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
19	RxFCSError	Receive Frame Check Sequence Error indicates the received frame incurred a FCS error (the frames FCS field did not match the FCS calculation performed over the frame DA through Data fields). RxFCSError is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
20	RxOversizedFrame	Receive Oversized Frame indicates the received frame was larger than the value set in the MaxFrameSize register. The entire frame is written into the RFD regardless of this error. RxOversizedFrame is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
21	RxLengthError	Receive Length Error indicates the received frame length differed from the length field in the Ethenet frame header. If the received frame is a runt, RxLengthError is a logic 0. RxLengthError is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
22	VLANDetected	VLAN Detected indicates the received Ethernet frame contains a VLAN tag. VLANDetected is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
23	TCPDetected	Transmission Control Protocol Detected indicates the received Ethernet frame contains TCP data within an Internet Protocol datagram. TCPDetected is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
24	TCPError	Transmission Control Protocol Error indicates the received Ethernet frame contains TCP data within an Internet Protocol datagram, and the TCP checksum calculation by the device did not match the checksm value in the TCP header. TCPError is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
25	UDPDetected	User Datagram Protocol Detected indicates the received Ethernet frame contains UDP data within an Internet Protocol datagram. UDPDetected is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
26	UDPError	User Datagram Protocol Error indicates the received Ethernet frame contains UDP data within an Internet Protocol datagram, and the UDP checksum calculation by the device did not match the checksum value in the UDP header. UDPError is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
27	IPDetected	Internet Protocol Detected indicates the received Ethernet frame contains an IP datagram. IPDetected is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.
28	IPError	Internet Protocol Error indicates the received Ethernet frame contains an IP datagram, and the IP checksum calculation by the device did not match the checksum value in the IP header. IPError is undefined (and should be ignored) unless the RFS FrameEnd field is a logic 1.

Bit	Bit Name	Bit Description
29	FrameStart	Frame Start indicates the first RFD used to describe a received Ethernet frame. In conjunction with the FrameEnd bit, these bits indicate the beginning and end of a single Ethernet frame within the RFD list. If both the Framestart and FrameEnd bits in the RFS field are a logic 1, the frame required only a single RFD.
30	FrameEnd	Frame End indicates the last RFD used to describe a received Ethernet frame. In conjunction with the FrameStart bit, these bits indicate the beginning and end of a single Ethernet frame within the RFD list. If both the FrameStart and FrameEnd bits in the RFS field are a logic 1, the frame required only a single RFD.
31	RFDDone	RFD Done is written as a logic 1 by the device after transferring received data to host system memory. If the device is directed to use (typically re-use) and RFD whose RFDDone bit is a logic 1, the device will not transfer data to the location indicated by the RFD (and thus will halt the receive DMA operation) until the RFDDone bit is a logic 0.
47..32	TCI	Tag Control Information contains the TCI portion of the VLAN tag found in the received frame described by this RFD (if a VLAN tag was found) regardless of the state of the MACCtrl register AutoVLANuntagging bit. TCI is only valid if the VLANDetected bit is a logic 1.
63..48	Reserved	Reserved for future use. Write as zero, ignore on read.

8.10.2.3 FragInfo

Class..... Receive DMA Data Structure
Base Address ..... RFD starting address in system memory
Address Offset 0x10
Access Mode ..... Read/Write
Width ..... 64 bits

Fragment Information indicates a block of contiguous system memory reserved for a portion, or for an entire received Ethernet frame. Fragments may be located anywhere in system memory, and need not be contiguous.

Bit	Bit Name	Bit Description
39..0	FragAddr	Fragment Address indicates the location within host system memory of the first byte of the data fragment. Fragments can be located anywhere within a 40 bit (1,099,511,627,776 or 1 Terabyte) memory space.
47..40	Reserved	Reserved for future use. Write as zero, ignore on read.
63..48	FragLen	Fragment Length indicates the length of the fragment in bytes. Fragments can range from zero to 64k (65,536) bytes in length.

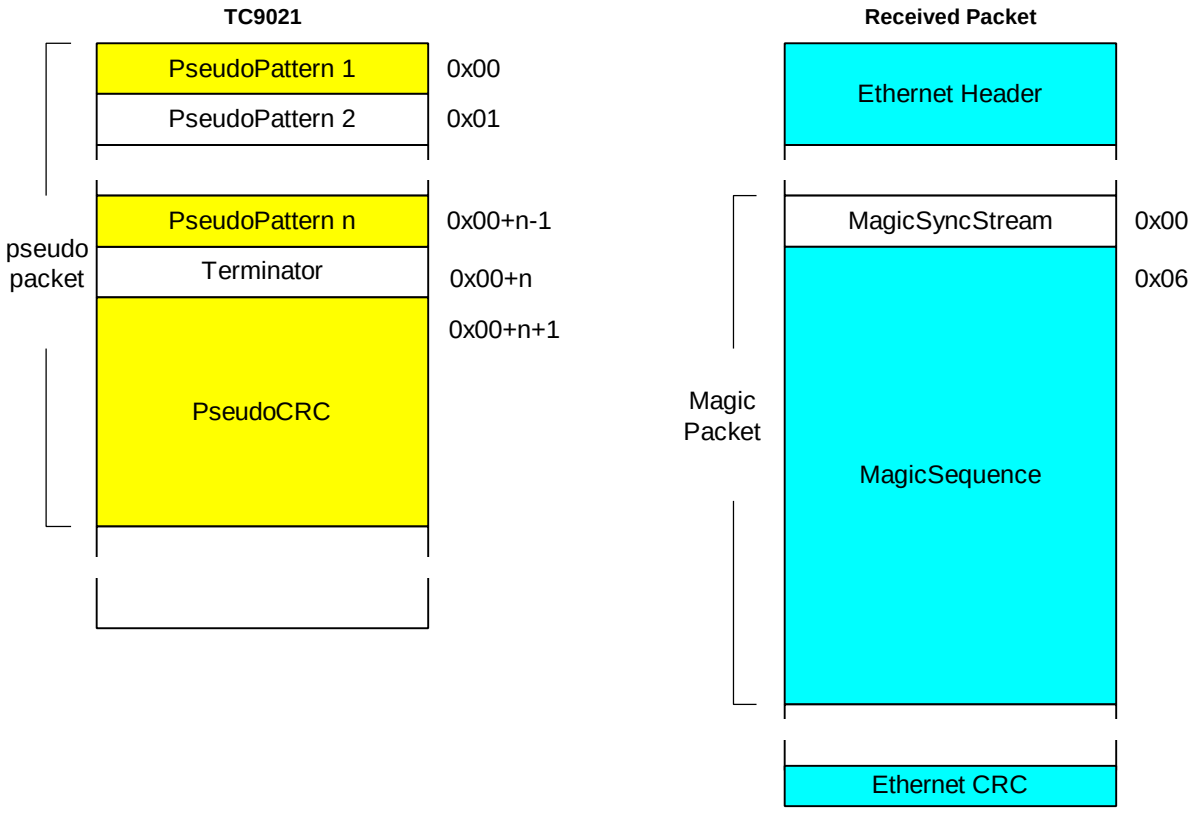
8.10.3 Wake Event Data Structures

The first Wake Event Data Structure is the Pseudo Packet. A Pseudo Packet is a set of patterns loaded into the device TxFIFO which specify bytes to be examined within received frames. A CRC is calculated over these bytes and compared with a CRC value supplied in the Pseudo Packet. If a match is found, the device issues a Wake Event. The matching technique may result in false wake events being reported to the host system. Each Pseudo Packet consists of one or more byte-offset/byte-count pairs (or Pseudo Patterns), a terminator symbol, and a 4-byte CRC value. The byte offsets within the Pseudo Patterns indicate the number of received frame bytes to be skipped in order to reach the next group of bytes to be included in the CRC calculation. The byte-counts within the Pseudo Patterns indicate the number of bytes in the next group to be included in the CRC calculation. The terminator indicates the end of the Pseudo Patterns for the Pseudo Packet. Immediately following the terminator is a 4-byte CRC. If there is another Pseudo Packet, it will immediately follow the CRC value.

The second Wake Event Data Structure is the Magic Packet. Magic Packets are uniquely formatted frames, which upon reception invoke a Wake Event by the device. Once the device has been placed in Magic Packet mode and put to sleep, it scans all incoming frames addressed to it for a data sequence

consisting of a synchronization stream followed immediately by 16 consecutive repetitions of the station's own 48-bit Ethernet MAC station address. The sequence can be located anywhere within the received frame.
The pseudo packet and Magic Packet data structures are shown in Figure 9.

FIGURE 9: Wake Event Data Structures, Pseudo Packet and Magic Packet



8.10.3.1 MagicSequence

Class..... Wake Event Data Structures, Magic Packet
Base Address ..... Start of Magic Packet
Address Offset 0x06
Access Mode ..... Read only
Width ..... 768 bits

Bit	Bit Name	Bit Description
767..0	MagicSequence	A sequence of 96 bytes, consisting of 16 consecutive, identical 6 bytes sequences, where each 6 byte sequence equals the station address of the station receiving the Magic Packet.

8.10.3.2 MagicSyncStream

Class..... Wake Event Data Structures, Magic Packet
Base Address ..... Start of Magic Packet
Address Offset 0x00
Access Mode ..... Read only
Width ..... 48 bits

Bit	Bit Name	Bit Description
47..0	MagicSyncStream	A stream of 6 bytes with the value 0xff indicates the start of the

Bit	Bit Name	Bit Description
		MagicSequence.

8.10.3.3 PseudoCRC

Class..... Wake Event Data Structures, Pseudo Packet
Base Address ..... Start of Pseudo Packet
Address Offset ..... 0x00+n+1 for n PseudoPatterns
Access Mode ..... Write only
Width ..... 32 bits
The 32-bit CRC as defined in the IEEE 802.3 Ethernet standard for the FCS, taken over the bytes (indicated by the PseudoPattern values) of a received frame.

Bit	Bit Name	Bit Description
7..0	PseudoCRCbyte0	The least significant byte of the PseudoCRC.
15..8	PseudoCRCbyte1	The second lest significant byte of the PseudoCRC.
23..16	PseudoCRCbyte2	The second most significant byte of the PseudoCRC.
31..24	PseudoCRCbyte3	The most significant byte of the PseudoCRC.

8.10.3.4 PseudoPattern

Class..... Wake Event Data Structures, Pseudo Packet
Base Address ..... Start of Pseudo Packet
Address Offset ..... 0x00 thru 0x00+n-1 for nth PseudoPattern
Access Mode ..... Write only
Width ..... 8 bits

Bit	Bit Name	Bit Description
3..0	ByteCount	ByteCount can take on a value of 0x0 to 0xe. A value of 0xf indicates an extended value. The extended value will occupy 8 bits and is contained in the next PseudoPattern. If both the ByteOffset and the ByteCount values are 0xf, the next PseudoPattern will be the extended ByeOffset, and the PseudoPattern after that will be the extended ByteCount.
7..4	ByteOffset	ByteOffset can take on a value of 0x0 to 0xe. A value of 0xf indicates an extended value. The extended value will occupy 8 bits and is contained in the next PseudoPattern. If both the ByteOffset and the ByteCount values are 0xf, the next PseudoPattern will be the extended ByteOffset, and the PseudoPattern after that will be the extended ByteCount.

8.10.3.5 Terminator

Class..... Wake Event Data Structures, Pseudo Packet
Base Address ..... Start of Pseudo Packet
Address Offset ..... 0x00+n for n PseudoPattern
Access Mode ..... Write only
Width ..... 8 bits

Bit	Bit Name	Bit Description
7..0	Terminator	A value of 0x00 indicates the end of the PseudoPattern.

8.10.4 RMON Statistics

The TC9021 implements a portion of the Remote Network Monitoring Management Information Base (RMON MIB) defined in RFC 1757. The Ethernet Statistics Group as defined in RFC 1757 is implemented via a set of TC9021 registers. Many Ethernet Statistics Group objects are implemented as dedicated registers which must be accessed using memory (not I/O) operations. A memory map of these dedicated RMON registers in shown in Table 7 .

TABLE 7: TC9021 RMON MIB Register Map

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
EtherStatsPkts1024to1518Octets				0x150
EtherStatsPkts512to1023Octets				0x14C
EtherStatsPkts256to511Octets				0x148
EtherStatsPkts128to255Octets				0x144
EtherStatsPkts65to127Octets				0x140
EtherStatsPkts64Octets				0x13C
EtherStatsPkts				0x138
EtherStatsOctets				0x134
EtherStatsJabbers				0x130
EtherStatsFragments				0x12C
EtherStatsUndersizePkts				0x128
EtherStatsCRCAlignErrors				0x124
EtherStatsPkts1024to1518OctetsTransmit				0x120
EtherStatsPkts512to1023OctetsTransmit				0x11C
EtherStatsPkts256to511OctetsTransmit				0x118
EtherStatsPkts128to255OctetsTransmit				0x114
EtheStatsPkts65to127OctetsTransmit				0x110
EtherStatsPkts64OctetsTransmit				0x10C
EtherStatsPktsTransmit				0x108
EtherStatsOctetsTransmit				0x104
EtherStatsCollisions				0x100

The remainder of the Ethernet Statistics Group objects are accessed via dual purpose statistic registers. A list of these dual purpose registers, and their RMON Ethernet Statistics equivalents is shown in Table 8.

Table 8: RMON MIB to TC9021 Register Equivalent Mapping

RMON MIB ETHERNET STATISTICS GROUP OBJECT	EQUIVALENT TC9021 STATISTIC REGISTER
EtherStatsDropEvents	FramesLostRxErrors
EtherStatsOversizePkts	FrameTooLongErrors
EtherStatsBroadcastPkts	BcstFramesRcvdOk
EtherStatsMulticastPkts	McstFramesRcvdOk
EtherStatsBroadcastPktsTransmit	BcstFramesXmtdOk
EtherStatsMulticastPktsTransmit	McstFramesXmtdOk

Note, RMON statistic objects with the “Transmit” suffix are not described specifically in RFC 1757, but are extensions of similar objects defined in RFC 1757 applied to transmit data.

8.10.4.1 EtherStatsCollisions

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x100

Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsCollisions	R/W	The best estimate of the total number of collisions on this Ethernet segment. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsCollisions reaches a value of 0xC000. EtherStatsCollisions is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsCollisions bit within the RMONStatistics Mask register.

8.10.4.2 EtherStatsCRCAlignErrors

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x124
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsCRCAlignErrors	R/W	The total number of packets received that had a length (excluding framing bits, but including FCS octets) of between 64 and 1518 octets, inclusive, but had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsCRCAlignErrors reaches a value of 0xC000. EtherStatsCRCAlignErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsCRCAlignErrors bit within the RMONStatisticsMask register.

8.10.4.3 EtherStatsFragments

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x12C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsFragments	R/W	The total number of packets received that were less than 64 octets in length (excluding framing bits but including FCS octets) and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). Note that it is entirely normal for EtherStatsFragments to increment. This is because it counts both runts (which are normal occurrences due to collisions) and noise hits. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsFragments reaches a value of

Bit	Bit Name	R/W	Bit Description
			0xC000. EtherStatsFragments is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsFragments bit within the RMONStatisticsMask register.

8.10.4.4 EtherStatsJabbers

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x130
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsJabbers	R/W	The total number of packets received that were longer than 1518 octets(excluding framing bits, but including FCS octets), and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a nonintegral number of octets (Alignment Error). Note that the above definition of jabber from RFC 1757 is different than the definition in IEEE-802.3. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsJabbers reaches a value of 0xC000. EtherStatsJabbers is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsJabbers bit within the RMONStatisticsMask register.

8.10.4.5 EtherStatsOctets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x134
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsOctets	R/W	The total number of octets of data (including those in bad packets) received on the network (excluding framing bits but including FCS octets). This object can be used as a reasonable estimate of Ethernet utilization. If greater precision is desired, the EtherStatsPkts and EtherStatsOctets objects should be sampled before and after a common interval. The differences in the sampled values are Pkts and Octets, respectively, and the number of seconds in the interval is Interval. These values are used to calculate the Utilization as follows: $\text{Utilization} = \frac{\text{Pkts}*(96+64)+(\text{Octets}*8)}{\text{Interval}*10{,}000{,}000}$ The result of this equation is the value Utilization which is the percent utilization of the Ethernet segment on a scale of 0 to 100 percent.

Bit	Bit Name	R/W	Bit Description
			All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception)the VLAN tag automatically. An UpdatesStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsOctets reaches a value of 0xC000. EtherStatsOctets is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsOctets/EtherStatsPkts bit within the RMONStatisticsMask register.

8.10.4.6 EtherStatsOctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x104
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsOctetsTransmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsOctetsTransmit reaches a value of 0xC000. EtherStatsOctetsTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsOctetsTransmit/EtherStatsPktsTransmit bit within the RMONStatisticsMask register.

8.10.4.7 EtherStatsPkts

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x138
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts	R/W	The total number of packets (including bad packets, broadcast packets, and multicast packets) received. Note, the ReceiveMode register settings will affect the results of EtherStatsPkts. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts reaches a value of 0xC000. EtherStatsPkts is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsOctets/EtherStatsPkts bit within the RMONStatistics-

Bit	Bit Name	R/W	Bit Description
			Mask register.

8.10.4.8 EtherStatsPkts64Octets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x13C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts64Octets	R/W	The total number of packets (including bad packets) received that were 64 octets in length (excluding framing bits but including FCS octets). All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts64Octets reaches a value of 0xC000. EtherStatsPkts64Octets is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts64Octets bit within the RMONStatisticsMask register.

8.10.4.9 EtherStatsPkts65to127Octets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x140
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts65to127 Octets	R/W	The total number of packets (including bad packets) received that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception)the VALN tag automatically. An UpdateStats interrup (UpdateStats bit within the IntStatus register)will occur when EtherStatsPkts65to127Octets reaches a value of oxC000. EtherStatsPkts65to127Octets is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts65to127Octets bit within the RMONStatisticsMask register.

8.10.4.10 EtherStatsPkts128to255Octets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value

Address Offset..... 0x144
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts 128to255Octets	R/W	The total number of packets (including bad packets) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStats Pkts128to255Octets reaches a value of 0xC000. EtherStatsPkts128to255Octets is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts128to255Octets bit within the RMONStatisticsMask register.

8.10.4.11 EtherStatsPkts256to511Octets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x148
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts256to511 Octets	R/W	The total number of packets (including bad packets) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts256to511Octets reaches a value of 0xC000. EtherStatsPkts256to511Octets is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts256to511Octets bit within the RMONStatisticsMask register.

8.10.4.12 EtherStatsPkts512to1023Octets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x14C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts512to102	R/W	The total number of packets (including bad packets) received that

Bit	Bit Name	R/W	Bit Description
	3Octets		were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception)the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts512to1023Octets reaches a value of 0xC000. EtherStatsPkts512to1023Octets is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts512to1023Octets bit within the RMONStatisticsMask register.

8.10.4.13 EtherStatsPkts1024to1518Octets

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x150
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts1024to1518Octets	R/W	The total number of packets (including bad packets) received that were between 1024 and 1518 octets in length inclusive (excluding framing bits but including FCS octets). All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception)the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts1024to1518Octets reaches a value of 0xC000. EtherStatsPkts 1024to1518Octets is enabled by writing a logic 1 to te StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts1024to1518Octets bit within the RMONStatisticsMask register.

8.10.4.14 EtherStatsPktsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x108
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPktsTransmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPktsTransmit reaches a value of 0xC000. EtherStatsPktsTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to

Bit	Bit Name	R/W	Bit Description
			the EtherStatsOctetsTransmit/EtherStatsPktsTransmit bit within the RMONStatisticsMask register.

8.10.4.15 EtherStatsPkts64OctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x10C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts64Octets Transmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission)or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts64OctetsTransmit reaches a value of 0xC000. EtherStatsPkts64OctetsTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts64OctetsTransmit bit within the RMONStatisticsMask register.

8.10.4.16 EtherStatsPkts65to127OctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x110
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts65to127 OctetsTransmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UupdateStats bit within the IntStatus register) will occur when EtherStatsPkts65to127OctetsTransmit reaches a value of 0xC000. EtherStatsPkts65to127OctetsTransmit is enabled by writing a logic 1 to the StatisticsEnalbe bit the MACCtrl register, and a logic 0 to the EtherStatsPkts65to127-OctetsTransmit bit within the RMONStatisticsMask register.

8.10.4.17 EtherStatsPkts128to255OctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O

Memory Base Address . MemBaseAddress register value
Address Offset 0x114
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts128to255 OctetsTransmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts128to255OctetsTransmit reaches a value of 0xC000. EtherStatsPkts128to255OctetsTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts128to255OctetesTransmit bit within the RMONStatisticsMask register.

8.10.4.18 EtherStatsPkts256to511OctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x118
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts256to511 OctetsTransmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts256to511OctetsTransmit reaches a value of 0xC000. EtherStatsPkts256to511OctetesTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts256to511OctetsTransmit bit within the RMONStatisticsMask register.

8.10.4.19 EtherStatsPkts512to1023OctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x11C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts512to1023OctetsTransmt	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrup (UpdateStats bit within the IntStatus register) will occur when EtherstatsPkts512to1023OctetsTransmit reaches a value of 0xC000. EtherStatsPkts512to1023OctetsTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts512to1023OctetsTransmit bit within the RMONStatisticsMask register.

8.10.4.20 EtherStatsPkts1024to1518OctetsTransmit

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x120
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsPkts1024to1518OctetsTransmit	R/W	An extension of the similar named object in RFC 1757 for transmit data as apposed to traditional RMON objects which record receive data. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when EtherStatsPkts1024to1518Octets -Transmit reaches a value of 0xC000. EtherStatsPkts1024to1518OctetsTransmit is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsPkts1024to1518OctetsTransmit bit within the RMONStatisticsMask register.

8.10.4.21 EtherStatsUndersizePkts

Class..... RMON Statistics
I/O Base Address ..... Not accessible via I/O
Memory Base Address . MemBaseAddress register value
Address Offset 0x128
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	EtherStatsUndersizePkts	R/W	The total number of packets received that were less than 64 Octets long (excluding framing bits, but including FCS octets) and were otherwise well formed. An UpdateStats interrupt (UpdateStats bit within the IntStatus

Bit	Bit Name	R/W	Bit Description
			register) will occur when EtherStatsUndersizePkts reaches a value of 0xC000. EtherStatsUndersizePkts is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the EtherStatsUndersizePkts bit within the RMONStatisticsMask register.

8.10.5 Ethernet MIB Statistics

The host interacts with the device mainly through slave registers, which occupy 256 bytes in the host system's I/O space, 512 bytes in memory space, or both. Generally, registers are referred to as "I/O registers", implying that the registers may in fact be mapped and accessed by the host system in memory space.

These registers must be accessed with instructions that are no larger than the bit-width of the register being accessed. There are several classes of I/O registers, with Ethernet Management Information Base (MIB) Statistics comprising a portion of the total I/O register space. The Ethernet MIB Statistic registers implement several counters defined in the IEEE 802.3 standard.

TABLE 9: TC9021 Ethernet MIB Statistics Register Map

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
FramesWEXDeferal		FramesAbortXSColls		FC
MacControlFramesCmtd		CarrierSenseErrors		F8
BcstFramesXmtdOk				F4
SingleColFrames				F0
MultiColFrames				EC
LateCollisions				E8
FramesWDeferredXmt				E4
McstFramesXmtdOk				E0
FramesXmtdOk				DC
BcstOctetXmtOk				D8
McstOctetXmtOk				D4
OctetXmtOk				D0
FramesLostRxErrors		FramesCheckSeqErrors		CC
InRangeLengthErrors		FrameTooLongErrors		C8
MacControlFramesRcvd				C4
				C0
BcstFramesRcvdOk				BC
McstFramesRcvdOk				B8
FramesRcvdOk				B4
BcstOctetRcvOk				B0
McstOctetRcvdOk				AC
OctetRcvOk				A8

8.10.5.1 BcstFramesRcvdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0xBE
Default Value 0x0000

Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	BcstFramesRcvdOk	R/W	Broadcast Frames Received OK is the count of the number of frames that are successfully received with destination address equal to the broadcast address (0Xffffffffffff). BcstFramesRcvdOk does not include frames received with frames too long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error (i.e. overrun).BcstFramesRcvdOk will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.22 An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when BcstFramesRcvdOk reaches a value of 0xC000. BcstFramesRcvdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the BcstFramesRcvdOk bit within the StatisticsMask register.

8.10.5.2 BcstFramesXmtdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0xF6
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	BcstFramesxmtdOk	R/W	Broadcast Frames Transmiited is the count of the number of frames that are successfully transmiited to the broadcast address (0xFFFFFFFFFFFF). Frames transmitted to other multicast addresses are excluded from this statistic. BcstFramesXmtdOk will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.19. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when BcstFramesXmtdOk reaches a value of 0xC000. BsctFramesXmtdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the BcstFramesXmtdOk bit within the StatisticsMask register.

8.10.5.3 BcstOctetRcvOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xB0
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	BcstOctetRcvOk	R/W	Broadcast Octets Received OK is the count of the number of data and padding octets in frames, with destination address equal to the broadcast address (0XFFFFFFFFFFFF), that are successful received. BcstOctetRcvOk does not include frames received with frames too long, FCS, length or alignment error, or frames lost due to internal MAC sublayer error (i.e. overrun).

Bit	Bit Name	R/W	Bit Description
			BcstOctetRcvOk will wrap around to zero after reaching 0xFFFFFFFF. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when BcstOctetRcvOk reaches a value of 0xC0000000. BcstOctetRcvOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the BcstOctetRcvOk bit within the StatisticsMask register.

8.10.5.4 BcstOctetXmtOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xD8
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	BcstOctetXmtOk	R/W	Broadcast Octets Transmitted OK is a count of data and padding octets of frames successfully transmitted to the broadcast address (0xFFFFFFFFFFFF). BcstOctetXmtOk will wrap around to zero after reaching 0xFFFFFFFF. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when BcstOctetXmtOk reaches a value of 0xC0000000. BcstOctetXmtOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the BcstOctetXmtOk bit within the StatisticsMask register.

8.10.5.5 CarrierSenseErrors

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xF8
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	CarrierSenseErrors	R/W	Carrier Sense Errors counts the number of times that the carrier sense signal (CRS) was de-asserted (a logic 0) during the transmission of a frame without collision. The carrier sense signal is not monitored for the purpose of this statistic until after the preamble and start-of-frame delimiter fields of the Ethernet frame have been transmitted. CarrierSenseErrors will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.13. An UpdateStats interrupt (UpdateStats bit within the IntStatus

Bit	Bit Name	R/W	Bit Description
			register) will occur when CarrierSenseErrors reaches a value of 0xC000. CarrierSenseErrors is enabled by writing a logic 1 to the Statistics Enable bit in the MACCtrl register, and a logic 0 to the CarrierSenseErrors bit within the StatisticsMask register.

8.10.5.6 FramesAbortXSColls

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xFC
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	FramesAbortXSColls	R/W	Frames Aborted Due to Excess Collisions counts the number of frames which are not transmitted successfully due to excessive collisions. FramesAbortXSColls will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.11. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FramesAbortXSColls reaches a value of 0xC000. FramesAbortXSColls is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesAbortXSColls bit within the StatisticsMask register.

8.10.5.7 FramesCheckSeqErrors

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0xCC
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	FramesCheckSeqErrors	R/W	Frame Check Sequence Errors is a count of received frames that are an integral number of octets in length and do not pass the FCS check. This does not include frames received with frame-too-long, or frame-too-short(runt) error. FramesCheckSeqErrors will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.6. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FramesCheckSeqErrors reaches a value of 0xC000. FramesCheckSeqErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesCheckSeqErrors bit within the StatisticsMask register.

8.10.5.8 FramesLostRxErrors

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0xCE
Default Value 0x0000
Access Rule..... Word

Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	FramesLostRxErrors	R/W	Frames Lost Due to Receive Errors is a count of the number of frames that should have been received (the destination address matched the filter criteria) but experienced a receive FIFO overrun error (the receive FIFO does not have enough free space to store the received data). FramesLostRxErrors only includes overruns that become apparent to the host system, and does not include frames that are completely ignored due to a completely full receive FIFO at the beginning of frame reception. FramesLostRxErrors will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.15. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FramesLostRxErrors reaches a value of 0xC000. FramesLostRxErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesLostRxErrors bit within the StatisticsMask register.

8.10.5.9 FramesRcvdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xB4
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	FramesRcvdOk	R/W	Frames Received OK is the count of the number of frames that are successfully received. FramesRcvdOk does not include frames received with frames too long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error (i.e. overrun). FramesRcvdOk will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.5. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FramesRcvdOk reaches a value of 0xC0000000. FramesRcvdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesRcvdOk bit within the StatisticsMask register.

8.10.5.10 FramesWDeferredXmt

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xE4
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	FramesWDeferredXmt	R/W	Frames with Deferred Transmit is a count of the number of frames that must delay their first attempt of transmission because the medium was busy. Frames involved in any collisions are not counted by FramesWDeferredXmt. FramesWDeferredXmt wrap

Bit	Bit Name	R/W	Bit Description
			around to zero after reaching 0xFFFFFFFF. See IEEE802.3 Clause 30.3.1.1.9. An UpdateStats interrupt (UpdateStats bit within the IntStaus register) will occur when FramesWDeferredXmt reaches a value of 0xC0000000. FramesWDeferredXmt is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesWDeferedXmt bit within the StatisticsMask register.

8.10.5.11 FramesWEXDeferal

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xFE
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	FramesWEXDeferal	R/W	Frames with Excessive Deferals counts the number of frames that deferred for an excessive period of time (exceeding the defer limit). FramesWEXDeferal is only incremented once per LLC frame. FramesWEXDeferal will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.20. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FramesWEXDeferal reaches a value of 0xC000. FramesWEXDeferal is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesWEXDeferal bit within the StatisticsMask register.

8.10.5.12 FramesXmtdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xDC
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	FramesXmtdOk	R/W	Frames Transmitted OK is a count of the number of frames that are successfully transmitted. FramesXmtdOk will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.2. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FramesXmtdOk reaches a value of 0xC0000000. FramesXmtdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FramesXmtdOk bit within the StatisticsMask register.

8.10.5.13 FrameTooLongErrors

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value

Address Offset 0xC8
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	FrameTooLongErrors	R/W	Frame Too Long Errors is a count of frames received whose length exceed the value in the MaxFrameSize register. FrameTooLongErrors will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Claruse 30.3.1.1.25. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when FrameTooLongErrors reaches a value of 0xC000. FrameTooLongErros is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the FrameTooLongErrors bit within the StatisticsMask register.

8.10.5.14 InRangeLengthErrors

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xCA
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	InRangeLengthErrors	R/W	In Range Length Errors is a count of the number of frames with the Length/Type field value between the minimum unpadded MAC client data size and the maximum allowed MAC client data size, inclusive, that does not match the number of MAC client data octets received. InRangeLengthErrors also increments for frames whose Length/Type field value is less than the minimum allowed unpadded MAC client data size, and the number of MAC client data octets received is greater than the minimum unpadded MAC client data size. InRangeLengthErrors will wrap around to zero after reaching 0xFFFF. See IEEE 802.3 Clause 30.3.1.1.23. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when InRangeLengthErrors reaches a value of 0xC000. InRangeLengthErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the InRangeLengthErrors bit within the StatisticsMask register.

8.10.5.15 LateCollisions

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xE8
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	LateCollisions	R/W	Late Collisions is a count of the number of times that a collision has been detected later than 1 slot time into the transmitted frame. LateCollisions will wrap around to zero after reaching

Bit	Bit Name	R/W	Bit Description
			0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.10. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when LateCollisions reaches a value of 0xC0000000. LateCollisions is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the LateCollisions bit within the StatisticsMask register.

8.10.5.16 MacControlFramesRcvd

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xC6
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	MacControlFramesRcvd	R/W	MAC Control Frames Received is a count of the number of MAC control PAUSE frames, and only PAUSE frames, received successfully. MacControlFramesRcvd will wrap around to zero after reaching 0xFFFF. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when MacControlFramesRcvd reaches a value of 0xC000. MacControlFramesRcvd is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the MacControlFramesRcvd bit within the StatisticsMask register.

8.10.5.17 MacControlFramesXmtd

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xFA
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	MacControlFramesXmtd	R/W	MAC Control Frames Transmitted is the count of MAC control frames transmitted by the TC9021. Note, MacControlFramesXmtd does not include MAC control frames transferred to the device by the host system via the transmit DMA process. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when MacControlFramesXmtd reaches a value of 0xC000. MacControlFramesXmtd is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the MacControlFramesXmtd bit within the StatisticsMask register.

8.10.5.18 McstFramesRcvdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value

Address Offset 0xB8
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	McstFramesRcvdOk	R/W	Multicast Frames Received OK is the count of the number of frames that are successfully received to a group destination address other than the broadcast address (0xFFFFFFFFFFFF). McstFramesRcvdOk does not include frames received with frames too long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error (i.e. overrun). McstFramesRcvdOk will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.21. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when McstFramesRcvdOk reaches a value of 0xC0000000. McstFramesRcvdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the McstFramesRcvdOk bit within the StatisticsMask register.

8.10.5.19 McstFramesXmtdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0xE0
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	McstFramesXmtdOk	R/W	Multicast Frames Transmitted OK is a count of the number of frames that are successfully transmitted to a group destination address other than the broadcast address (OxFFFFFFFFFFFF). McstFramesXmtdOk will wrap around to zero after reaching OxFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.18. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when McstFramesXmtdOk reaches a value of 0xC0000000. McstFramesXmtdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to McstFramesXmtdOk bit within the StatisticsMask register.

8.10.5.20 McstOctetRcvdOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0xAC
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	McstOctetRcvdOk	R/W	Multicast octets Received OK is the count of the number of data and padding octets in frames, to a group destination address other than the broadcast address (0xFFFFFFFFFFFF), that are successfully received. McstOctetRcvdOk does not include frames

Bit	Bit Name	R/W	Bit Description
			received with frames too long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error(i.e. overrun). McstOctetRcvdOk will wrap around to zero after reaching 0xFFFFFFFF. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when McstOctetRcvdOk reaches a value of 0xC0000000. McstOctetRcvdOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the McstOctetRcvdOk bit within the StatisticsMask register.

8.10.5.21 McstOctetXmtOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xD4
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	McstOctetXmtOk	R/W	Multicast Octets Transmitted OK is a count of data and padding octets of frames successfully transmitted to a group destination address other than the broadcast address (0xFFFFFFFFFFFF). McstOctetXmtOk will wrap around to zero after reaching 0xFFFFFFFF. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octetes) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when McstOctetXmtOk reaches a value of 0xC0000000. McstOctetXmtOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the McstOctetXmtOk bit within the StatisticsMask register.

8.10.5.22 MultiColFrames

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xEC
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	MultiColFrames	R/W	Multiple Collision Frames is a count of the number of frames that are involved in more than one collision and are subsequently transmitted successfully. MultiColFrames will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.4.

Bit	Bit Name	R/W	Bit Description
			An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when MultiColFrames reaches a value of 0xC0000000. MultiColFrames is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the MultiColFrames bit within the StatisticsMask register.

8.10.5.23 OctetRcvOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xA8
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	OctetRcvOk	R/W	Octets Received OK is the count of the number of data and padding octets in frames that are successfully received. OctetRcvOk does not include frames received with frames too long, FCS, length or alignment errors, or frames lost due to internal MAC sublayer error (i.e. overrun). OctetRcvOk will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.14. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when OctetRcvOk reaches a value of 0xC0000000. OctetRcvOk is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the OctetRcvOk bit within the StatisticsMask register.

8.10.5.24 OctetXmtOk

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xD0
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	OctetXmtOk	R/W	Octets Transmitted OK is a count of data and padding octets of frames successfully transmitted. OctetXmtOk will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.8. All TC9021 byte and octet count based statistic registers include the VLAN tag (4 octets) regardless of whether or not the device is adding (on frame transmission) or removing (on frame reception) the VLAN tag automatically. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when OctetXmtOk reaches a value of 0xC0000000. OctetXmtOk is enabled by writing a logic 1 to the

Bit	Bit Name	R/W	Bit Description
			StatisticsEnable bit in the MACCtrl register, and a logic 0 to the OctetXmtOk bit within the StatisticsMask register.

8.10.5.25 SingleColFrames

Class..... Ethernet MIB Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xF0
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
31..0	SingleColFrames	R/W	Single Collision Frames is a count of the number of frames that are involved in a single collision, and are subsequently transmitted successfully. SingleColFrames will wrap around to zero after reaching 0xFFFFFFFF. See IEEE 802.3 Clause 30.3.1.1.3. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when SingleColFrames reaches a value of 0xC0000000. SingleColFrames is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the SingleColFrames bit within the StatisticsMask register.

8.10.6 I/O Registers

The host interacts with the device mainly through slave registers, which occupy 256 bytes in the host system's I/O space, 512 bytes in memory space, or both. Generally, registers are referred to as "I/O registers", implying that the registers may in fact be mapped and accessed by the host system in memory space.

These registers must be accessed with instructions that are no larger than the bit-width of the register being accessed. There are several classes of I/O registers including Statistic, Control and Status, DMA, ASIC, and Interrupts.

TABLE 10: TC9021 I/O Register Map

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
				FC
				F8
		TxJumboFrames		F4
				F0
				EC
				E8
				E4
				E0
				DC
				D8
				D4
				D0
				CC
				C8
		UDPCheckSumErrors		C4

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
IPCheckSumErrors		TCPCheckSumErrors		C0
		RxJumboFrames		BC
				B8
				B4
				B0
				AC
				A8
				A4
				A0
StatisticsMask				9C
RMONStatisticsMask				98
				94
HashTable[63:32]				90
HashTable[31:0]				8C
		ReceiveMode		88
MaxFrameSize				84
	VLANId			80
VLANHashTable		StationAddress[47:32]		7C
StationAddress[31:0]				78
	PhyCtrl			74
VLANTag				70
MACCtrl				6C
				68
				64
TxStatus				60
IntStatus		IntEnable		5C
IntStatusAck				58
Countdown				54
		WakeEvent	ExpRomData	50
ExpRomAddr				4C
EepromCtrl		EepromData		48
		TxStartThresh		44
				40
FlowOnThresh		FlowOffThresh		3C
RxEarlyThresh		FIFOCtrl		38
				34
AsicCtrl				30
		DebugCtrl		2C
RxDMAIntCtrl				28
	RxDMAPollPeriod	RxDMAUrgentThresh	RxDMABurstThresh	24
RFDListPtr[63:32]				20
RFDListPtr[31:0]				1C

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
	TxDMAPollPeriod	TxDMAUrgentThresh	TxDMABurstThresh	18
TFDListPtr[63:32]				14
TFDListPtr[31:0]				10
				0C
Reserved(RxDMAStatus)				08
				04
DMACtrl				00

8.10.6.1 AsicCtrl

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x30
Default Value 0x00006100
Access Rule..... Word, Double Word
Width ..... 32 bits
The contents of bits 7 through 0 of AsicCtrl are read from EEPROM at reset.

Bit	Bit Name	R/W	Bit Description
0	Reserved (ExpRomDisable)	N/A	Reserved for future use. Write as zero, ignore on read. (This bit, when set, disables accesses to the on-adapter Expansion ROM. This bit is included to allow bypassing the Expansion ROM without having to physically remove it from the board. When this bit is set, the device responds to any read in its configured Expansion ROM space by returning 00000000h, and it ignores writes to the Expansion ROM. This bit resets to 0.)
1	ExpRomSize	R/W	Expansion Read Only Memory Size. ExpRomsize specifies the size of the Expansion ROM to be used with the device. **Bit 1** **Expansion Rom Size(KB)** 0 32 1 64
2	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
3	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
4	PhySpeed10	R	Physical Layer Speed 10Mbps. When PhySpeed10 is a logic 1, 10Mbps operation is available from the PHY device interfaced to the device. When PhySpeed10 is a logic 0 the PHY device interfaced to the device is not 10Mbps capable.
5	PhySpeed100	R	Physical Layer Speed 100Mbps. When PhySpeed100 is a logic 1, 100Mbps operation is available from the PHY device interfaced to the device. When PhySpeed100 is a logic 0 the PHY device interfaced to the device is not 100Mbps capable.
6	PhySpeed1000	R	Physical Layer Speed 1000Mbps. When PhySpeed1000 is a logic 1, 1000Mbps operation is available from the PHY device interfaced to the device. When PhySpeed1000 is a logic 0 the

Bit	Bit Name	R/W	Bit Description
			PHY device interfaced to the device is not 1000Mbps capable.
7	PhyMedia	R	Physical Layer Media. PhyMedia indicates the media type of the PHY device interfaced to the device. When PhyMedia is a logic 1, the PHY device is utilizing fiber media. When PhyMedia is a logic 0, the PHY device is utilizing twisted-pair media. The combination of PhyMedia, PhySpeed100, and PhySpeed1000 will determine the capability of the PHY device interfaced to the device. **PhyMeida** **PhySpeed1000** **PhySpeed100** **PHY Device interfaced to the TC9021** 0 0 0 Undefined 0 0 1 100BASE-T 0 1 0 1000BASE-T 0 1 1 100BASE-T or 1000BASE-T 1 0 0 Undefined 1 0 1 100BASE-F 1 1 0 1000BASE-SX/LX 1 1 1 100BASE-F or 1000BASE-SX/LX

Bit	Bit Name	R/W	Bit Description
10..8	ForcedConfig	R/W	Forced Configuration. ForcedConfig is used to enable and select a Forced Configuration mode for the device. Forced Configuration mode is targeted toward embedded applications which do not utilize an EEPROM. In Forced Configuration mode, the device is accessed via a PCI bus without first performing PCI configuration or loading parameters from an EEPROM. The ForcedConfig bits 10 through 8 are latched (with a logic inversion) from signal pins ED bits 2 through 0 respectively upon termination of a device reset. **Bit 10** **Bit 9** **Bit 8** **Forced Configuration Mode** 0 0 0 None 0 0 1 1 0 1 X Reserved 1 X X Reserved (alternate Deviceld and Vendorld used) In Forced Configuration mode 1, the device is configured as follows: I/O base address=0x200 I/O target cycles=enabled Memory target cycles=disabled Bus master cycles=enabled Expansion ROM cycles=disabled
11	D3ResetDisable	R/W	D3 Power State Reset Disable. When D3ResetDisable is a logic 1 the device is configured for operation in a Wake-On-LAN environment (see section 8.5). When D3ResetDisable is a logic 1 and the device is in the D3 power state, assertion of RSTN signal pin will not reset the device, assertion of the RSTN signal will not reset the device.
12	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
13	SpeedupMode	R/W	Speed Up Mode. SpeedupMode is used for simulation purposes only. When SpeedupMode is a logic 1, the device operation is modified to decrease simulation time. SpeedupMode is latched (with a logic inversion) from signal pins ED bit 5 upon termination of a device reset.

Bit	Bit Name	R/W	Bit Description
14	LEDMode	R/W	Light Emitting Diode Mode. LEDMode is used to control the LED signal pin functionality. When LEDMode is a logic 0 the LED signal pins operate in LED MODE 0. when LEDMode is a logic 1 the LED signal pins operate in LED mode 1 Note, when LED signals alternate between logic 1/0, they alternate over a 41.89ms period, where the logic 0 (or LED ON) state persists for 5.24ms and the logic 1 (or LED OFF) state persists for 36.65ms. **LED Signal Pin** **Mode 0** **Mode 1** EA2/LEDPWRN Continuous logic 0 when power is applied. Alternating logic 1/0 when frame transmission in progress. Continuous logic 0 when power is applied. EA1/LEDLNK1000N Continuous logic 0 when Ethernet link is valid. Alternating logic 1/0 when frame reception in progress. Continuous logic 0 when Ethernet link is valid. Alternating logic 1/0 when frame reception or transmission in progress. EA0/LEDDPLXN Continuous logic 0 when the TC9021 is configured for full duplex operation. Alternating logic 1/0 when the device detects a collision. Continuous logic 0 when the TC9021 is configured for full duplex operation. Continuous logic 1 when the device is configured for half duplex operation.
15	RstOutPolarity	R/W	Reset Output Polarity. RstOutPolarity affects the polarity of the RSTOUT signal. When RstOutPolarity is a logic 1 the RSTOUT signal will assert HIGH to indicate a reset is in progress. When RstOutPolarity is a logic 0 the RSTOUT signal will assert LOW to indicate a reset is in progress.
16	GlobalReset	W	Global Reset. When GlobalReset is a logic 1, the device resets all of the logic functions and registers specified by the DMA, FIFO, Network, Host, AutoInit, and RstOut bits (related to both the transmit and receive processes as applicable). GlobalReset is self-clearing, and requires that the device RMONStatistics, Ethernet MIB Statistics, and I/O Registers be reinitialized. The PCI Configuration Registers are not affected by GlobalReset.
17	RxReset	W	Receive Reset. When RxReset is a logic 1 the device resets all of the receive logic functions and registers specified by the DMA, FIFO, Network, Host, and AutoInit bits. RxReset is self-clearing, and should not be used after initialization except to recover from receive errors such as a receive FIFO over run.
18	TxReset	W	Transmit Reset. When TxReset is a logic 1 the device resets all of the transmit logic functions and registers specified by the DMA, FIFO, Network, Host, and AutoInit bits. TxReset is self clearing, and is required to be used after a transmit underrun error.
19	DMA	W	DMA Reset. DMA selects (when a logic 1) excludes (when a logic 0) the device DMA functions and registers for/from reset based on the value of the GlobalRest, RxReset, and TxReset bits.

Bit	Bit Name	R/W	Bit Description
			The DMA bit is self-clearing. **DMA Function/Register** **Reset On TxReset** **Reset On RxReset** **Reset On GlobalReset** Transmit DMA logic X X Receive DMA logic X X TFDListPtr register X X RFDListPtr register X X TxDMAComplete bit in the DMACtrl register X X RxDMAComplete bit in the DMACtrl register X X TxDMAInProg bit in the DMACtrl register X X RxEarlyDisable bit in the DMACtrl register X X
20	FIFO	W	FIFO Reset. FIFO selects (when a logic 1) or excludes (when a logic 0) the device FIFO functions and registers for/from reset based on the value of the GlobalReset, RxReset, and TxReset bits. The FIFO bit is self-clearing. **FIFO Function/Register** **Reset On TxReset** **Reset On RxReset** **Reset On GlobalReset**

Bit	Bit Name	R/W	Bit Description
			Transmit FIFO logic X X Receive FIFO logic X X TxStartThresh register X X RxEarlyThresh register X X
21	Network	W	Network Reset. Network selects (when a logic 1) or excludes (when a logic 0) the device network functions and registers for/from reset based on the value of the GlobalReset, RxReset, and TxReset bits. The Network bit is self-clearing. **NETWORK Function/Register** **Reset On TxReset** **Reset On RxReset** **Reset On GlobalReset** Transmit network interface logic X X Receive network interface logic X X Transmit MAC register X X Receive MAC register X X TxStatus register X X

Bit	Bit Name	R/W	Bit Description
			Receive-Mode register X X All RMON Statistics and Ethernet MIB Statistics registers X X
22	Host	W	Host Reset. Host selects (when a logic 1) or excludes (when a logic 0) the device host bus interface logic functions and registers for/from reset based on the value of the GlobalReset bit. The Host bit is self-clearing. **HOST Function/Register** **RESET on GlobalReset** Host bus interface logic X IntStatus register X IntEnable register X Countdown register X Transmit and receive DMA functions X
23	AutoInit	W	Automatic Initialization Reset. AutoInit selects (when a logic 1) or excludes (when a logic 0) the device auto-initialization logic function for/from re-loading device parameters from an EEPROM based on the value of the GlobalReset bit. The AutoInit bit is self-clearing.
24	RstOut	W	Reset Out Assert. RstOut selects (when a logic 1) or excludes (when a logic 0) the device RSTOUT signal for/from assertion (as determined by the RstOutPolarity bit) based on the value of the GlobalReset bit. The RstOut bit is self-clearing.
25	InterruptRequest	W	Interrupt Request. When InterruptRequest is a logic 1, the IntRequested bit of the IntStatus register is set to a logic 1. InterruptRequest is self-clearing.
26	ResetBusy	R	Reset Busy. When ResetBusy is a logic 1 a reset process is in progress. After asserting a reset using the GlobalReset, RxReset, or TxReset bits, the ResetBusy bit must be polled (or periodically read) until it is a logic 0 indicating the reset operation is complete.
31..27	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.2 CountDown

Class..... I/O Registers, Interrupt

I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x54
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits
Countdown is a programmable, decrementing counter which will generate an interrupt upon expiration (reaching a value of 0x0000).

Bit	Bit Name	R/W	Bit Description
15..0	Count	R/W	Count. Count is the current value of Countdown register. When Count reaches 0x0000, it continues to decrement, wrapping to 0xFFFF.
2..16	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
24	CountdownSpeed	R/W	Count Down Speed. When operating at 1000Mbps and CountdownSpeed is a logic 0, the interval between decrements of the Countdown register is 3200 ns. When operating at 1000Mbps and CountdownSpeed is a logic 1, the interval between decrements of the Countdown register is 320 ns. When operating at 100Mbps or 10Mbps, the state of CountdownSpeed has no effect on the Countdown register interval. When operating at 100Mbps or 10Mbps, the interval between decrements of the Countdown register is 3200 ns.
25	CountdownMode	R/W	Count Down Mode. When CountdownMode is a logic 0, the Countdown register begins decrementing when a nono-zero value is written to the Countdown register. When CountdwonMode is a logic 1, the Countdown register begins decrementing after the TxDMAComplete bit in the IntStatus register is a logic 1.
26	CountdownIntEnabled	R	Count Down Interrupt Enabled. When CountdownIntEnabled is a logic 0, expiration of the Countdown timer will not set the IntRequested bit of the IntStatus register. When CountdownIntEnabled is a logic 1, expiration of the Countdown register will set the IntRequested bit in the IntStatus register. A logic 0 is written to CountdownIntEnabled when the IntRequested bit in the IntStatus register is a logic 1, or when a value of 0x0000 is written into the Count field. A logic 1 is written to CountdownIntEnabled when a non-zero value is written into the Count field.
31..27	Rserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.3 DebugCtrl

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x2C
Default Value 0x000C
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
0	GPIO0Ctrl	R/W	General Purpose Input Output 0 Control. GPIO0Ctrl specifies the direction of the EA6/GPIO0 signal. When GPIO0Ctrl is a logic 0, the EA6/GPIO0 signal is an input. When GPIO0Ctrl is a logic 1, the EA6/GPIO0 signal is an output.
1	GPIO1Ctrl	R/W	General Purpose Input Output 1 Control. GPIO1Ctrl specifies the

Bit	Bit Name	R/W	Bit Description
			direction of the EA7/GPIO1 signal. When GPIO1Ctrl is a logic 0, the EA7/GPIO1 signal is an input. When GPIO1Ctrl is a logic 1, the EA7/GPIO1 signal is an output.
2	GPIO0	R/W	General Purpose Input Output 0. GPIO0 represents the value of EA6/GPIO0 signal regardless of the state of GPIO0Ctrl. If GPIO0Ctrl is a logic 0, writes to GPIO0 are ignored.
3	GPIO1	R/W	General Purpose Input Output 1. GPIO1 represents the value of the EA7/GPIO1 signal regardless of the state of GPIO1Ctrl. If GPIO1Ctrl is a logic 0, writes to GPIO1 are ignored.
4	dbDisableDnHalt	R/W	For testing purposes only.
5	dbDisableUpHalt	R/W	For testing purposes only.
6	dbWrSameFSH	R/W	For testing purposes only.
7	dbNearEmpty	R/W	For testing purposes only.
8	dbSyncContrDone	R/W	For testing purposes only.
9	dbFrCurDoneAck	R/W	For testing purposes only.
10	dbFrcSpd1000	R/W	Force Speed to 1000Mbps when a logic 1 will cause the register access logic to behave as if the AsicClk speed is 62.5MHz.
15..11	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.4 DMACtrl

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x00
Default Value 0x00000000
Access Rule..... Word or Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
2..0	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
3	RxDMAComplete	R	Receive DMA Complete. RxDMAComplete is identical to the RxDMAComplete bit in the IntStatus register. RxDMAComplete is a logic 0 when the receive DMA process for a received Ethernet frame begins. RxDMAComplete is a logic 0 also when the RxDMAComplete interrupt is acknowledged.
4	RxDMAPollNow	W	Receive DMA Poll Now. When RxDMAPollNow is a logic 1 a “poll now” command is issued to the receive DMA process. The “poll now” receive DMA command resets the receive DMA poll timer which forces the current RFD RFDNxetPtr and RFS fields to be read. RxDMAPollNow is a self clearing.
7..5	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
10..8	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
11	TxDMAComplete	R	Transmit DMA Complete. TxDMAComplete is identical to the TxDMAComplete bit in the IntStatus register. TxDMAComplete is a logic 0 when the TxDMAComplete interrupt is acknowledged.
12	TxDMAPollNow	W	Transmit DMA Poll Now. When TxDMAPollNow is a logic 1 a “poll now” command is issued to the transmit DMA process. The “poll now” transmit DMA command resets the transmit DMA poll timer which forces the current TFD TFDNextPtr and TFC fields to be read. TxDMAPollNow is a self clearing.

Bit	Bit Name	R/W	Bit Description
13	Reserved	N/A	Reserved for future use. Write as zero
14	Reserved	N/A	Reserved for future use. Write as zero
15	TxDMAInProg	R	Transmit DMA In Progress. When TxDMAInProg is a logic 1 a transmit DMA operation is in progress. TxDMAInProg is primarily used for underrun recovery processes which must wait for TxDMAInProg to be a logic 0 before issuing a transmit reset via the TxReset bit of the AsicCtrl register.
16	RxEarlyDisable	R/W	Receive Early Disable. RxEarlyDisable is used in conjunction with the RxEarlyThresh register to determine the start of receive DMA processes on received Ethernet frames. If a receive DMA bus-master arbitration does not begin based on the conditions of the RxEarlyThresh register, then the start of the receive DMA process depends on the state of RxEarlyDisable. When RxEarlyDisable is a logic 0, the receive DMA process will begin bus-master arbitration when 60 bytes of the received Ethernet frame are present in the receive FIFO. When RxEarlyDisable is a logic 1, the receive DMA process will begin bus-master arbitration when the entire frame is present in the receive FIFO.
17	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
18	MWIDisable	R/W	Memory Write Invalidate Disable. When MWIDisable is a logic 1, the bus master logic will not use the PCI Memory Write Invalidate (MWI) command.
19	TxWriteBackDisable	R/W	Transmit Write Back Disable. When TxWriteBackDisable is a logic 1 the device will not update the TFDDone bit and will not poll the TFDDone bit within the TFC field following a transmit DMA operation. When TxWriteBackDisable is a logic 0 the device will update the TFDDone bit for and will poll the TFDDone bit within the TFC field following each transmit DMA operation.
22..20	TxBurstLimit	R/W	Transmit Burst Limit. TxBurstLimit indicates the number of TFD FragInfo fields the device will transfer at a time. The valid range of values is 0x1, 2, 3, 4, and 5. All non-valid values will be interpreted as the value 0x1. TxBurstLimit is a system dependent parameter which should be set such to a value corresponding to the number of fragments present in the majority of Ethernet frames. In many systems, most Ethernet frames consist of 3 of less fragments, which implies a TxBurstLimit of 3.
29..23	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
30	TargetAbort	R	Target Abort. TargetAbort is a logic 1 when the device experiences a target abort sequence when operating as a bus master. TargetAbort indicates a fatal error and must be cleard before further transmit or receive DMA operation can proceed. TargetAbort is cleard via the AsicCtrl register GlobalReset/Host bits.
31	MasterAbort	R	Master Abort. MasterAbort is a logic 1 when the device experisences a master abort sequence when operating as a bus master. MasterAbort indicate a fatal error, and must be cleard before further transmit or receive DMA operation can proceed. MasterAbort is cleared via the AsicCtrl register GlobalReset/Host bits.

8.10.6.5 EepromCtrl

Class..... I/O Registers, Control and Status

I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x4A
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

EepromCtrl provides the host with a method for issuing commands to the TC9021's serial EEPROM controller. Individual 16-bit word locations within the EEPROM may be written, read or erased. Also, the EEPROM's WriteEnable, WriteDisable, EraseAll and WriteAll commands can be issued. Two-bit opcodes and 8-bit addresses are written to this register to cause the device to carry out the desired EEPROM command. If data is to written to the EEPROM, the 16-bit data word must be written to EepromData by the host prior to issuing the associated write command. Similarly, if data is to be read from the EEPROM, the read data will be available via EepromData register. The EEPROM is a particularly slow device. It is important that the host wait until the EepromBusy bit is a logic 0 before issuing a command to EepromCtrl.

Bit	Bit Name	R/W	Bit Description
7..0	EepromAddress	R/W	EEPROM Address. EepromAddress identifies one of the 256 sixteen-bit words to be the target for the ReadRegister, WriteRegister and EraseRegister EEPROM commands. Bits 7 and 6 are further define EEPROM sub-commands based on the value of EepromOpcode. Bits 7 and 6 of EepromAddress define a sub-command only if EepromOpcode is 0x0. **Bit 7** **Bit 6** **SUB-Command** 0 0 WriteDisable 0 1 WriteAll 1 0 EraseAll 1 1 WriteEnable
9..8	EepromOpcode	R/W	EEPROM Operation Code. EepromOpcode specifies one of three individual commands and a single group of our sub-commands. **Bit 9** **Bit 8** **OPCODE Command** 0 0 Write Enable/Disable & Write/Erase all sub-commands 0

Bit	Bit Name	R/W	Bit Description
			1 WriteRegister 1 0 ReadRegister 1 1 EraseRegister
14..10	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
15	EepromBusy	R	EEPROM Busy. EepromBusy is a logic 1 during the execution of EEPROM commands. Further commands should not be issued to EepromCtrl nor should data be read from EepromData while EepromBusy is a logic 1.

8.10.6.6 EepromData

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x48
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	EepromData	R/W	EepromData is a 16-bit data register for use with the adapter's serial EEPROM. Data from the EEPROM can be read by the host from EepromData register after the EepromBusy bit in the EepromCtrl register is a logic 0. Data to be written to the EEPROM is written to EepromData prior to issuing the write command to EepromCtrl.

8.10.6.7 ExpRomAddr

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x4C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
15..0	ExpRomAddr	R/W	Expansion ROM Address. ExpRomAddr holds the address to be used for direct I/O accesses of the Expansion ROM through the ExpRomData port. To access a byte in the Expansion ROM, write the address of the byte to be accessed into ExpRomAddr. Then issue either a read or a write to ExpRomData. For reads, the ROM value will be returned by the read instruction. For writes, the new value will be programmed into the ROM upon completion of the write instruction.
31..16	Reserved	N/A	Reserved for future use. Write as zero, Ignore on read.

8.10.6.8 ExpRomData

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x50
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	ExpRomData	R/W	Expansion ROM Data. ExpRomData is the data port for performing direct I/O byte-wide accesses of the Expansion ROM. A read of ExpRomData returns the ROM byte value from the location specified by ExpRomAddr. A write to ExpRomData causes the write data to be programmed into the ROM location specified by ExpRomAddr.

8.10.6.9 FIFOCtrl

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x38
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits
The bits in this register provide various control and indications of TxFIFO and RxFIFO diagnostic.

Bit	Bit Name	R/W	Bit Description
0	RAMTestMode	R/W	Random Access Memory Test Mode. When RAMTestMode is a logic 1 indicates the FIFO RAM is in the test mode. Ransom Access Memory Test Mode is also entered if bit 3 of the ED bus is a logic 0 during reset.
13..1	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
14	Transmitting	R	Transmitting. When Transmitting is a logic 1 indicates the MAC logic is transmitting or waiting to transmit (deferring).
15	Receiving	R	Receiving. When Receiving is a logic 1 indicates the device is receiving a frame into the receive FIFO.

8.10.6.10 FlowOffThresh

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x3C
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
10..0	FlowOffThresh	R/W	Flow Off Threshold. FlowOffThresh sets a watermark within the receive FIFO. If the amount of occupied space (measured in 16 byte increments) within the receive FIFO falls below the value set in the FlowOffThresh register, a PAUSE MAC Control frame with pause_time set to 0x0000 is transmitted. Only one PAUSE

Bit	Bit Name	R/W	Bit Description
			frame is transmitted when the FlowOffThresh watermark is crossed (see section 8.7.3).
	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.11 FlowOnThresh

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x3E
Default Value 0x07FF
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
10..0	FlowOnThresh	R/W	Flow On Threshold. FlowOnThresh sets a watermark within the receive FIFO. If the amount of occupied space (measured in 16 byte increments) within the receive FIFO exceeds the value set in the FlowOnThresh register, a PAUSE MAC Control frame with pause_time set to 0xFFFF (or 65,535*512ns=33.553ms) is transmitted. Only one PAUSE frame is transmitted when the FlowOnThresh watermark is crossed (see section 8.7.3).
15..11	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.12 HashTable

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x8C
Default Value 0x0000000000000000
Access Rule..... Double Word
Width ..... 64 bits

Bit	Bit Name	R/W	Bit Description
63..0	HashTable	R/W	Hash Table holds a 64-bit value used for selectively receiving multicast frames. Setting the ReceiveMulticastHash bit in the ReceiveMode register enables the filtering mechanism. The hash table is cleared upon reset, and must be properly set by the host. The device applies a cyclic-redundancy-check (the same CRC used to calculate the frame data FCS) to the destination address of all incoming multicast frames (Ethernet frames with multicast bit set in their destination address field). The least significant 6 bits of the CRC result are used as an addressing index into the hash table. If the HashTable bit addressed by the index is a logic 1, the frame is accepted by the device and transferred to higher layers. If the HashTable bit addressed by the index is a logic 0, the frame is discarded.

8.10.6.13 IntEnable

Class..... I/O Registers, Interrupt
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x5C
Default Value 0x0000
Access Rule..... Word

Width ..... 16 bits
IntEnable enables individual interrupts as specified in the IntStatus register. Setting a bit in IntEnable will allow the corresponding interrupt source to generate an interrupt on the PCI bus. IntEnable is cleared by a read of IntStatusAck register.

Bit	Bit Name	R/W	Bit Description
0	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
1	EnHostError	R/W	Enables the HostError bit in the IntStatus register to generate an interrupt.
2	EnTxComplete	R/W	Enables the TxComplete bit in the IntStatus register to generate an interrupt.
3	EnMACControlFrame	R/W	Enables the MACControlFrame bit in the IntStatus register to generate an interrupt.
4	EnRxComplete	R/W	Enables the RxComplete bit in the IntStatus register to generate an interrupt.
5	EnRxEarly	R/W	Enables the RxEarly bit in the IntStatus register to generate an interrupt.
6	EnInRequested	R/W	Enables the IntRequested bit in the IntStatus register to generate an interrupt.
7	EnUpdateStats	R/W	Enables the UpdateStats bit in the Intstatus register to generate an interrupt.
8	EnLinkEvent	R/W	Enables the LinkEvent bit in the IntStatus register to generate an interrupt.
9	EnTxDMAComplete	R/W	Enables the TxDMAComplete bit in the IntStatus register to generate an interrupt.
10	EnRxDMAComplete	R/W	Enables the RxDMAComplete bit in the IntStatus register to generate an interrupt.
11	EnRFDListEnd	R/W	Enables the RFDListEnd bit in the IntStatus register to generate an interrupt.
12	EnRxDMAPriority	R/W	Enables the RxDMAPriority bit in th IntStatus register to generate an interrupt.
15..13	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.14 IntStatus

Class..... I/O Registers, Interrupt
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x5E
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits
IntStatus indicates the source of interrupts and indications on the device.

Bit	Bit Name	R/W	Bit Description
0	InterruptStatus	R/W	Interrupt Status. InterruptStatus is a logic 1 when the device is driving the bus interrupt signal. It is a logical OR of all the interrupt-causing bits after they have been filtered through the IntEnable register.
1	HostError	R/W	Host Error. HostError is a logic 1 when a catastrophic error related to the bus interface occurs. The conditions which set HostError are PCI target abort and PCI master abort. HostError is cleared by setting the GlobalReset and Host bits in the AsicCtrl register. If HostError is a logic 1, and the EnHostError bit in the IntEnable register is also a logic 1, an interrupt will be generated.

Bit	Bit Name	R/W	Bit Description
2	TxComplete	R/W	Transmit Complete. TxComplete is a logic 1 when a frame (whose TFC field TxIndicate bit is a logic 1) has been successfully transmitted or for any frame that experiences an error during transmit. The TxComplete interrupt is acknowledged by reading the TxStatus register. If TxComplete is a logic 1, and the EnTxComplete bit in the IntEnable register is also a logic 1, an interrupt will be generated.
3	MACControlFrame	R/W	MAC Control Frame. MACControlFrame is a logic 1 when a MAC Control frame has been received by the device. MACControlFrame is acknowledged by writing a logic 1 to MACControlFrame. If MACControlFrame is a logic 1, and the EnMACControlFrame bit in the IntEnable register is also a logic 1, an interrupt will be generated.
4	RxComplete	R/W	Receive Complete. RxComplete is a logic 1 when one or more entire frames have been received into the receive FIFO. RxComplete is automatically acknowledged by the RxDMALogic as it transfers frames. If RxComplete is a logic 1. and the EnRxComplete bit in the IntEnable register is also a logic 1, an interrupt will be generated. The host system should disable the RxComplete interrupt and mask RxComplete when reading IntStatus.
5	RxEarly	R/W	Receive Early. RxEarly is a logic 1 when the number of bytes of a frame which is being received is greater than the value of the RxEarlyThresh register. When the frame has been completely received by the device, RxEarly will be a logic 0 and RxComplete will be a logic 1. RxEarly is acknowledged by writing a logic 1 to RxEarly. If RxEarly is a logic 1, and the EnRxEarly bit in the IntEnable register is also a logic 1, an interrupt will be generated.
6	IntRequested	R/W	Interrupt Requested. IntRequested is a logic 1 when the host system requested an interrupt by setting the InterruptRequest bit in the AsicCtrl register or when the Countdown register expires. IntRequested is acknowledged by writing a logic 1 to IntRequested. If IntRequested is a logic 1, and the EnInRequested bit in the IntEnable register is also a logic 1, an interrupt will be generated.
7	UpdateStats	R/W	Update Statistics. UpdateStats is a logic 1 when one or more of the statistics counters (RMON Statistics, Ethernet MIB statistics, or I/O Registers Statistics) is nearing an overflow condition (typically 75% of the statistic register's maximum value). The host system should respond to an UpdateStats interrupt by reading all of the statistic registers, thereby acknowledging and clearing UpdateStats bit. If UpdateStats is a logic 1, and the EnUpdateStats bit in the IntEnable register is also a logic 1, an interrupt will be generated.
8	LinkEvent	R/W	Link Event. LinkEvent is a logic 1 when there is a transition of PHYLNK10N signal (i.e. change in the link status of the PHY device). LinkEvent is acknowledged by writing a logic 1 to LinkEvent. If LinkEvent is a logic 1, and the EnLinkEvent bit in the IntEnable register is also a logic 1, an interrupt will be generated.
9	TxDMAComplete	R/W	Transmit DMA Complete. TxDMAComplete is a logic 1 when a frame transfer via transmit DMA has completed, and the TFD in associated with the transmit DMA operation had the it's TFC

Bit	Bit Name	R/W	Bit Description
			TxDMAIndicate bit set to a logic 1. TxDMAComplete is acknowledged by writing a logic 1 to TxDMAComplete. To determine which frame(s) have been transferred to the device via transmit DMA, the host may examine the TFDDone bits in the TFC fields of each TFD in the TFDList (see section 8.3.1 for more details). If TxDMAComplete is a logic 1, and the EnTxDMAComplete bit in the IntEnable register is also a logic 1, an interrupt will be generated.
10	RxDMAComplete	R/W	Receive DMA Complete. RxDMAComplete is a logic 1 when a frame transfer via receive DMA has completed. RxDMAComplete is acknowledged by writing a logic 1 to RxDMAComplete. Based on the configuration of the RxDMAIntCtrl register, RxDMAComlete interrupts may occur for each RFD which is transferred to the device, or only after multiple RFDs have been transferred (see section 8.3.4 for more details). If RxDMAComplete is a logic 1, and the EnRxDMAComplete bit in the IntEnable register is also a logic 1, an interrupt will be generated.
11	RFDListEnd	R/W	RFD List End. RFDListEnd is a logic 1 when the RxDMA Logic has reached the end of the RFD list (as indicated by a logic 1 in the RFDDone bit in the RFS field, and a 0x0000000000000000 value in the RFDNextPtr field of the RFD). RFDListEnd is acknowledged by writing a 1 to RFDListEnd. If RFDListEnd is a logic 1, and the EnRFDListEnd bit in the IntEnable register is also a logic 1, an interrupt will be generated.
12	RxDMAPriority	R/W	Receive DMA Priority. RxDMAPriority is a logic 1 when an Ethernet frame has been received with a priority tag of equal or higher priority than the value set in the PriorityThresh field of the RxDMAIntCtrl register. RxDMAPriority is acknowledged by writing a 1 to RxDMAPriority. If RxDMAPriority is a logic 1, and the EnRxDMAPriority bit in the IntEnable register is also a logic 1, an interrupt will be generated.
15..13	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.15 IntStatusAck

Class..... I/O Registers, Interrupt
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x5A
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

IntStatusAck is another version of the IntStatus register, having the same bit definition as IntStatus, but providing additional functionality to reduce the number of I/O operations required to perform common tasks related to interrupt handling. In addition to returning the IntStatus value for the specified interrupt, when read IntStatusAck also acknowledges the TxDMAComplete, RxDMAComplete, RFDListEnd, RxEarly, IntRequested, MACControlFrame, RxDMAPriority, and LinkEvent bits within the IntStatus register (if they are set), and clears the IntEnable register preventing subsequent events from generating an interrupt.

Bit	Bit Name	R/W	Bit Description
0	InterruptStatus	R/W	See description in IntStatus register description.
1	HostError	R/W	See description in IntStatus register description.
2	TxComplete	R/W	See description in IntStatus register description.
3	MACControlFrame	R/W	See description in IntStatus register description.
4	RxComplete	R/W	See description in IntStatus register description.
5	RxEarly	R/W	See description in IntStatus register description.
6	IntRequested	R/W	See description in IntStatus register description.
7	UpdateStats	R/W	See description in IntStatus register description.
8	LinkEvent	R/W	See description in IntStatus register description.
9	TxDMAComplete	R/W	See description in IntStatus register description.
10	RxDMAComplete	R/W	See description in IntStatus register description.
11	RFDListEnd	R/W	See description in IntStatus register description.
12	RxDMAPriority	R/W	See description in IntStatus register description.
15..13	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.16 IPCheckSumErrors

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xC2
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	IPChecksumErrors	R/W	IP Check sum Errors is a count of received frames which contain IP datagrams, which fail the IP checksum as defined in RFC 791. IPCheckSumErrors will wrap around to zero after reaching 0xFFFF. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when IPCheckSumErrors reaches a value of 0xC000. IPCheckSumErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic to the IPCheckSumErrors bit within the StatisticsMask register.

8.10.6.17 MACCtrl

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x6C
Default Value 0x00000000
Access Rule..... Word, Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
1..0	IFSSelect	R/W	Inter-Frame Spacing. IFSSelect indicates the minimum number of bit times between the end of one Ethernet frame, and the beginning of another when the device is deferring after a collision with the device the last device to successfully acquire the network (in half duplex mode). By selecting a large value for IFSSelect,

Bit	Bit Name	R/W	Bit Description
			the device will become less “aggressive” on the network and may defer more often (preventing the device from “capturing” the network). The performance of the device may decrease as the IFSSelect value is increased from the standard value. **Bit 1** **Bit 0** **INTER-Frame spacing in bit times** 0 0 96 (802.3 standard value, and default) 0 1 1024 1 0 1792 1 1 4352
4..2	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
5	DuplexSelect	R/W	Duplex Select. DuplexSelect configures the device to function in half or full duplex mode. If DuplexSelect is a logic 0, the device operates in half duplex mode. If DuplexSelect is a logic 1, the device operates in full duplex mode. In full duplex mode the transmitter deference to receive traffic functionality is disabled, allowing simultaneous receive and transmit traffic. Full duplex operation has the side-effect of disabling the CarrierSenseErrors statistic register. Following a change to DuplexSelect, the device transmit and receive functions must be reset by setting the AsicCtrl register TxReset and RxReset bits both to a logic 1.
6	Reseved (RcvLargeFrames)	R/W	Reserved for future use. Write as zero, ignore on read. (This bit determines the frame size at which the OversizedFrame error is generated for receive frames When RcvLargeFrames is cleared, minimum OversizedFrame size is 1514 bytes. When RcvLargeFrames is set, minimum OversizedFrame size is 4491 bytes. (This value was the maximum FDDI frame size of 4500 bytes, subtracting bytes for fields that have no Ethernet equivalent.) The frame size at which an OversizedFrame error will be flagged includes the destination and source addresses, the type/length field, and the FCS field.)
7	TxFlowControlEnable	R/W	Transmit Flow Control Enable. When TxFlowControlEnable is a logic 1 the receive FIFO threshold values defined in FlowOnThresh and FlowOffThresh registers are used to determine automatic transmission of PAUSE frames by the device. It is the responsibility of the host system to assure that if TxFlowControlEnable is a logic 1, the MACCtrl register DuplexSelect bit must also be a logic 1.

Bit	Bit Name	R/W	Bit Description
8	RxFlowControlEnable	R/W	Receive Flow control enable. When RxFlowControlEnable is a logic 0 the device will treat all incoming frames (even PAUSE frames) as data, and will not take any action if a PAUSE frame is received. When RxFlowControlEnable is a logic 1, receive flow control is enabled and the device will act upon incoming flow control PAUSE frames. It is the responsibility of the host system to assure that if RxFlowControlEnable is a logic 1, the MACCtrl register DuplexSelect bit must also be a logic 1.
9	RcvFCS	R/W	Receive Frame Check Sequence. When RcvFCS is a logic 1 the receive frame's FCS field is passed to the host as part of the data in the receive FIFO. The state of RcvFCS does not affect the device's checking of the frame's FCS field and posting of the FCS error status. The value of RcvFCS should only be changed during initialization of the device.
10	FIFOLoopback	R/W	FIFO Loopback. When FIFOLoopback is a logic 1 the device will apply data from the output of the transmit FIFO directly to the input of the receive FIFO. When using FIFOLoopback, it is the host system's responsibility to ensure that the proper interframe spacing by not loading more than one trasmit frame at a time into the transmit FIFO. Following a change to the FIFOLoopback bit, the device transmit and receive functions must be reset by setting the AsicCtrl register TxReset and RxReset bits both to a logic 1.
11	MACLoopback	R/W	Media Access Control Loopback. When MACLoopback is a logic 1 the device will apply transmit data at the output of the Media Access Control (MAC)logic transmit interface to the MAC receive interface. Following a change to the MACLoopback bit, the device transmit and receive functions must be reset by setting the AsicCtrl register TxReset and RxReset bits both to a logic 1.
12	AutoVLANtagging	R/W	Automatic VLAN Tagging. When AutoVLANtagging is a logic 1 the device will apply a VLAN tag as specified by the VLANTag register to every Ethernet frame prior to transmission. A logic 0 indicates the device should not insert a VLAN tag.
13	AutoVLANuntagging	R/W	Automatic VLAN Tag Removal. When AutoVLANuntagging is a logic 1 the device will remove the VLAN tag (if any) in all received Ethernet frames. A logic 0 indicates the device should not remove VLAN tags from received frames.
15..14	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
16	CollisionDetect	R	Collision Detect. CollisionDetect provides a real-time indication of the state of the COL signal within the device.
17	CarrierSense	R	Carrier Sense. CarrierSense provides a real-time indication of the state of the CRS signal within the device.
20..18	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
21	StatisticsEnable	W	Statistics Enable. When StatisticsEnable is a logic 1 the device will increment the various statistics counters and registers as applicable. StatisticsEnable is self-clearing.
22	StatisticsDisable	W	Statistics Disable. When StatisticsDisable is a logic 1 the device will not increment any statistics registers. The values in the statistics registers will remain unchanged. StatisticsDisable is self-clearing.
23	StatisticsEnabled	R	Statistics Enabled. When StatisticsEnabled is a logic 1 the statistic registers will increment as applicable.
24	TxEnable	W	Transmit Enable. When TxEnable is a logic 1 the transmitter logic is enabled. TxEnable is self-clearing.
25	TxDisable	W	Transmit disable. When TxDisable is a logic 1 the transmitter

Bit	Bit Name	R/W	Bit Description
			logic is disabled. TxDisable is self-clearing.
26	TxEnabled	R	Transmit Enabled. When TxEnabled is a logic 1 the transmitter is enabled.
27	RxEnable	W	Receive Enable. When RxEnable is a logic 1 the receive logic is enabled. RxEnable is self-clearing.
28	RxDisable	W	Receive Disable. When RxDisable is a logic 1 the receive logic is disabled. RxDisable is self-clearing.
29	RxEnabled	R	Receive Enabled. When RxEnabled is a logic 1 the receive logic is enabled.
30	Paused	R	Paused. When Paused is a logic 1 a PAUSE MAC Control frame has been received and caused the transmit MAC logic to halt for the duration of the pause_time value specified in the PAUSE frame. Paused is cleared when MAC transmission resumes.
31	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.18 MaxFrameSize

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x86
Default Value 0x05EA
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
13..0	MaxFrameSize	R/W	Maximum Frame Size indicates the maximum expected size (in bytes) of received Ethernet frames measured from the start of the Destination Address field, to the end of the Data field. If the number of bytes in a receive frame is equal to or greater that the value in the MaxFramesize register (or the value in the MaxFrameSize register plus 4 bytes for received frames with VLAN tages), the RxOversizedFrame bit in the RFS field of the current RFD is a logic 1.
15..14	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.19 PhyCtrl

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x76
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

PhyCtrl contains control bits for the GMII Management Interface. The GMII Management Interface is used to access registers in a GMII PHY device or the TC9021 1000BASE-X PCS management registers. The Management Interface is a two-wire serial interface connecting TC9021 to any GMII compliant PHY devices residing in the system. The host system operates the Management Interface by writing and reading bit patterns to PhyCtrl which correspond to the physical wave forms required on the interface signals. For more information on the Management Interface signal protocols, refer to the Media Independent Interface standard of IEEE 802.3u Specification. For reference, the timing parameters of the MDC and MDIO signals from the IEEE specification, Clause 22.2.11, and 22.3.4 are given in Table 11.

TABLE 11: MgmtClk/MgmtData Timing Requirements

PARMETER	VALUE	UNITS
MDC minimum low time	160	ns
MDC minimum high time	160	ns
MDC minimum period	400	ns
MDIO to MDC minimum setup time (when MDIO is driven by the TC9021)	10	ns
MDIO to MDC minimum hold time (when MDIO is driven by the TC9021)	10	ns
MDIO to MDC maximum delay time (when MDIO is driven by an internal PCS or external PHY)	300	ns

Bit	Bit Name	R/W	Bit Description
0	MgmtClk	R/W	GMII Management Clock. MgmtClk directly drives the management clock, either the internal MDC signal to the PCS layer, or the MDC/EWRAP signal to external PHY device(s).
1	MgmtData	R/W	GMII Management Data Bit. When the MgmtDir bit is a logic 1, the value written to MgmtData is driven onto the MDIO signal. When MgmtDir is a logic 0, data driven by the PHY device can be read from MgmtData.
2	MgmtDir	R/W	GMII Management Data Direction. Setting MgmtDir causes device to drive MDIO with the data bit written into MgmtData.
3	PhyDuplexPolarity	R/W	PHY Duplex Polarity. When PhyDuplexPolarity is a logic 0 the PHYDPLXN input pin is active low.
4	PhyDuplexStatus	R	PHY Duplex Status. PhyDuplexStatus provides a real-time indication of the duplex status of the PHY. If PhyDuplex Status is a logic 1, the PHY is operating in full duplex mode.
5	PhyLnkPolarity	R/W	PHY link Polarity. When PhyLnkPolarity is a logic 0 the PHYLNK10N, PHYLNK100N, and PHYLNK1000N input pins are active low.
7..6	LinkSpeed	R	PHY Link Speed/Status. LinkSpeed provides a real-time indication of the link status of the PHY. **Bit 7** **Bit 6** **Link speed/status** 0 0 Link down (default). 0 1 Link up at 10Mbps 1 0 Link up at 100Mbps 1 1 Link up at 1000Mbps

8.10.6.20 ReceiveMode

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x88
Default Value 0x00
Access Rule..... Word
Width ..... 16 bits
Each bit in ReceiveMode, when set, enables reception of a different type of frame.

Bit	Bit Name	R/W	Bit Description
0	ReceiveUnicast	R/W	Receive Unicast Frames when a logic 1 enables the device to receive unicast frames that match the 48-bit value in the StationAddress register of the device.
1	ReceiveMulticast	R/W	Receive Multicast Frames when a logic 1 enables the device to receive all multicast frames, including broadcast.
2	ReceiveBroadcast	R/W	Receive Broadcast Frames when a logic 1 enables the device to receive all broadcast frames.
3	ReceiveAllFrames	R/W	Receive All Frames when a logic 1 enables the device to receive all frames promiscuously.
4	ReceiveMulticastHash	R/W	Receive Multicast Frames Using Hash Table, when a logic 1 enables the device to receive frames that pass the hash filtering mechanism defined in the HashTable register.
5	ReceiveIPMulticast	R/W	Receive IP Multicast Frames when a logic 1 enables the device to receive all multicast IP datagrams, which are mapped into Ethernet multicast frames with destination address of 01:00:5e:xx:xx:xx as defined in RFC 1112 and RFC 1700. The first 3 bytes require exact match, and the last 3 bytes are ignored.
7..6	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
8	ReceiveVLANMatch	R/W	Receive Frames With Matching VLAN Tags when a logic 1 indicates the device will filter (or drop) receive frames which do not match one of the VLAN tags specified in the VLANId register. Before verifying VLAN tags, all receive frames must pass the filtering specified by the ReceiveUnicast, ReceiveMulticast, ReceiveBroadcast, ReceiveAllFrames, ReceiveMulticastHash, and ReceiveIPMulticast bit configurations.
9	ReceiveVLANHash	R/W	Receive Frames Using VLAN Tag Hash Table, enables the device filter (or drop) receive frames which do not pass the hash filtering mechanism defined in the VLANHashTable register. Before verifying VLAN tags, all receive frames must pass the filtering specified by the ReceiveUnicast, ReceiveMulticast, ReceivBroadcast, ReceiveAllFrames, ReceiveMulticastHash, and ReceiveIPMulticast bit configurations.
15..10	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.21 RFDListPtr

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x1C
Default Value 0x0000000000000000
Access Rule..... Double Word
Width ..... 64 bits

Bit	Bit Name	R/W	Bit Description
39..0	RFDListptr	R/W	RFD List Pointer. RFDListPtr holds the physical address within host system memory of the current RFD in the RFD list. A value of 0x0000000000000000 for RFDListPtr indicates that no more RFDs are available to accept received Ethernet frame data. RFDListptr can only specify host system memory addresses which are on 8-byte boundaries (i. e. bits 2 through 0 must be 0), therefore RFDs must be aligned on 8-byte physical address boundaries. RFDListptr must be written directly by the host system initially to indicate the head of a newly created RFD list and is subsequently updated by the device as it processes RFDs in the RFD list. As the device finishes processing a RFD, it loads RFDListPtr with the value from the current RFD's RFDNextPtr field. If the device reads a value of 0x0000000000000000 from the current RFD's RFDNextPtr field, the receive DMA process enters the polling state, waiting for a non-zero value to be written to current RFD's RFDNextPtr.
63..40	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.22 RMONStatisticsMask

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x98
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
0	EtherStatsCRCAlignErrors	R/W	EtherStatsCRCAlignErrors Mask when a loigic 1 indicates the EtherStatsCRCAlignErrors RMON statistic register will not increment.
1	EtherStatsUndersizePkts	R/W	EtherStatsUndersizePkts Mask when a logic 1 indicates the EtherStatsUndersizePkts RMON statistic register will not increment.
2	EtherStatsFragments	R/W	EtherStatsFragments Mask when a logic 1 indicates the EtherStatsFragments RMON statistic register will not increment.
3	EtherStatsJabbers	R/W	EtherStatsJabbers Mask when a logic 1 indicates the EtherStatsJabbers RMON statistic register will not increment.
4	EtherStatsOctets/EtherStatsPkts	R/W	EtherStatsOctets/EtherStatsPkts Mask when a logic 1 indicates the EtherStatsOctets and EtherStatsPkts RMON statistic registers will not increment.
5	EtherStatsPkts64Octets	R/W	EtherStatsPkts64Octets mask when a logic 1 indicates the EtherStatsPkts64Octets RMON statistic register will not increment.
6	EtherStatsPkts65to127Octets	R/W	EtherStatsPkts65to127Octets Mask when a logic 1 indicates the EtherStatsPkts65to127Octets RMON statistic register will not increment.
7	EtherStatsPkts128to255Octets	R/W	EtherStatsPkts128to255Octets Mask when a logic 1 indicates the EtherStatsPkts128to255Octets RMON statistic register will not increment.
8	EtherStatsPkts256to511octets	R/W	EtherStatsPkts256to511Octets Mask when a logic 1 indicates the EtherStatsPkts256to511Octets RMON statistic register will not increment.
9	EtherStatsPkts512to102	R/W	EtherStatsPkts512to1023Octets Mask when a logic 1 indicates the

Bit	Bit Name	R/W	Bit Description
	3Octets		EtherStatsPkts512to1023Octets RMON statistic register will not increment.
10	EtherStatsPkts1024to1518Octets	R/W	EtherStatsPkts1024to1518Octets Mask when a logic 1 indicates the EtherStatsPkts1024to1518octets RMON statistic register will not increment.
11	EtherStatsCollisions	R/W	EtherStatsCollisions Mask when a logic 1 indicates the EtherStatsCollisions RMON statistic register will not increment.
12	EtherStatsOctetsTransmit/EtherStatsPktsTransmit	R/W	EtherStatsOctetsTransmit/EtherStatsPktsTransmit Mask when a logic 1 indicates the EtherStatsOctetsTransmit and EtherStatsPktsTransmit RMON statistic registers will not increment.
13	EtherStatsPkts64OctetsTransmit	R/W	EtherStatsPkts64OctetsTransmit Mask when a logic 1 indicates the EtherStatsPkts64OctetsTransmit RMON statistic register will not increment.
14	EtherStatsPkts65to127OctetsTransmit	R/W	EtherStatsPkts65to127OctetsTransmit Mask when a logic 1 indicates the EtherStatsPkts65to127OctetsTransmit RMON statistic register will not increment.
15	EtherStatsPkts128to255OctetsTransmit	R/W	EtherStatsPkts128to255OctetsTransmit Mask when a logic 1 indicates the EtherStatsPkts128to255OctetsTransmit RMON statistic register will not increment.
16	EtherStatsPkts256to511OctetsTransmit	R/W	EtherStatsPkts256to511OctetsTransmit Mask when a logic 1 indicates the EtherStatsPkts256to511OctetsTransmit RMON statistic register will not increment.
17	EtherStatsPkts512to1023OctetsTransmit	R/W	EtherStatsPkts512to1023OctetsTransmit Mask when a logic 1 indicates the EtherStatsPkts512to1023OctetsTransmit RMON statistic register will not increment.
18	EtherStatsPkts1024to1518OctetsTransmit	R/W	EtherStatsPkts1024to1518OctetsTransmit Mask when a logic 1 indicates the EtherStatsPkts1024to1518OctetsTransmit RMON statistic register will not increment.
31..19	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.23 RxDMABurstThresh

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x24
Default Value 0x08
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	RxDMABurstThresh	R/W	Receive DMA Burst Threshold. RxDMABurstThresh sets the threshold by which the device determines when to assert receive DMA bus master requests. The threshold is specified based on the amount of occupied space in the receive FIFO in increments of 32 bytes. When the number of bytes in the receive FIFO occupied by receive data rises above the value specified by RxDMABurstThresh, the device may make a receive DMA request on the PCI bus. If the number of bytes in the receive FIFO occupied by receive data exceeds the value in the FragLen sub field of the FragInfo field of the current RFD, the device will make receive DMA bus request regardless of the value in RxDMABurstThresh. The maximum value of RxDMABurstThresh is 0xFF, or 8192

Bit	Bit Name	R/W	Bit Description
			bytes (256*32=8192). The minimum value of RxDMABurstThresh is 0x08, or 256 bytes, and any smaller value is interpreted as 0x08.

8.10.6.24 RxDMAIntCtrl

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x28
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

The RxDMAIntCtrl register is used for configuring the receive DMA interrupt coalescing feature of the device (see section 8.3.4). Receive DMA interrupts may be coalesced (that is grouped such that a single interrupt is issued to indicate multiple Ethernet frames have been received) and the frequency of receive DMA interrupts can be set based on either the number of Ethernet frames received (via the RxFrameCount field), or after a fixed amount of time following receipt of an Ethernet frame (via the RxDMAWaitTime field). It is not possible to completely disable the assertion of receive DMA interrupts if a receive DMA operation has taken place. If a receive DMA operation has completed, a RxDMAComplete interrupt will be asserted for based on either condition described by the RxDMAIntCtrl register, whichever occurs first.

Bit	Bit Name	R/W	Bit Description
7..0	RxFrameCount	R/W	Receive Frame Count. RxFrameCount Indicates the maximum number of frames which will be transferred via a receive DMA transfer before the RxDMAComplete bit in the IntStatus register is set to a logic 1 (a RxDMAComplete interrupt). The minimum value of RxFrameCount is 0x01 (which indicates a RxDMAComplete interrupt will occur for every receive DMA transfer), and any smaller value is interpreted as 0x01.
9..8	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
12..10	PriorityThresh	R/W	Priority Threshold. PriorityThresh holds the value which is compared to the Priority field within received Ethernet frames which contain Tag Control Information (TCI) fields in the frame header. If a received Ethernet frame contains a TCI field with a priority value equal to or greater than the value in PriorityThresh, the RxDMAPriority bit in the IntStatus register is set to a logic 1 (a RxDMAPriority interrupt). **PriorityThresh Field Bit** **Ethernet Frame TCI Priority Field Bit** 12 8 11 7 10 6
15..13	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
31..16	RxDMAWaitTime	R/W	Receive DMA Wait Time. RxDMAWaitTime indicates the

Bit	Bit Name	R/W	Bit Description
			maximum amount of time (in 64ns increments) between completion of a receive DMA transfer operation and setting of the RxDMAComplete bit in the IntStatus register to a logic 1 (a RxDMAComplete interrupt). A value of 0x0000 indicates a RxDMAComplete interrupt will occur immediately following each receive DMA transfer.

8.10.6.25 RxDMAPollPeriod

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x26
Default Value 0xFF
Access Rule..... Byte
Width ..... 8 bits.

Bit	Bit Name	R/W	Bit Description
7..0	RxDMAPollPeriod	R/W	Receive DMA Poll Period. RxDMAPollPeriod determines the rate at which the current RFD in the receive DMA process is read for changes in the RFDNextPtr and RFS fields. RxDMAPollPeriod is specified in 320 ns increments. The maximum value is 256 (or 81.92 us). The minimum valid value is 0x01. Since RxDMAPollPeriod cannot be set to 0x00, polling is always in effect during receive DMA operation.

8.10.6.26 Reserved(RxDMAStatus)

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x08
Access Rule..... Double Word
Default Value 0x00000000
Width ..... 32 bits

Receive DMA Status shows the status of various operations in the receive DMA process. Reserved(RxDMAStatus) should be read only while the receive DMA process is in the polling state (see section 8.2.2). The format of this register is identical to that of the RFS field of a RFD. The contents of Reserved(RxDMAStatus) are written into the RFS field of the current RFD upon completion of the receive DMA process.
For bit definitions, see 8.10.2.2 bits 0 through 31.

8.10.6.27 RxDMAUrgentThresh

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x25
Default Value 0x04
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	RxDMAUrgentThresh	R/W	Receive DMA Urgent Threshold. RxDMAUrgentThresh sets the threshold by which the device determines when to assert receive urgent DMA bus master requests. The threshold is specified based on the amount of unoccupied space in the receive FIFO in

Bit	Bit Name	R/W	Bit Description
			increments of 32 bytes. When the number of bytes in the receive FIFO not occupied by receive data falls below the value specified by RxDMAUrgentThresh, the device may make an urgent receive DMA request on the PCI bus. The maximum value of RxDMAUrgentThresh is 0xFF, or 8192 bytes (256*32=8192). The minimum value of RxDMAUrgentThresth is 0x04, or 128 bytes, and any smaller value is interpreted as 0x04.

8.10.6.28 RxEarlyThresh

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x3A
Default Value 0x07FF
Access Rule..... Word
Width ..... 16 bits.

Bit	Bit Name	R/W	Bit Description
10..0	RxEarlyThresh	R/W	Receive Early Threshold. RxEarlyThresh defines the number of quad-words (64 bits) of an Ethernet frame (beginning with the Destination Address field) which must be received before a RxEarly interrupt is issued, and before the start of the receive DMA process. If the RxEarlyDisable bit in DMACtrl register is a logic 1, the receive DMA process for a frame will not begin until the number of quad-words indicated by RxEarlyThresh have been received The minimum value of RxEarlyThresh is 0x01, any value smaller than this will be interpreted as 0x01.
15..1	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.29 RxJumboFrames

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xBC
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	RxJumboFrames	R/W	Jumbo Frames Received is a count of the number of frames received successfully whose frame length (measured from the Destination Address field to the end of the Frame Check sequence field) is greater than 1518 bytes (1522 bytes for VLAN tagged frames). RxJumboFrames will wrap around to zero after reaching 0xFFFF. An Updatestats interrupt (UpdateStats bit within the IntStatus register) will occur when RxJumboFrames reaches a value of 0xC000. RxJumboFrames is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the RxJumboFrames bit within the StatisticsMask register.

8.10.6.30 StationAddress

Class..... I/O Registers, Control and Status

I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x78
Default Value 0x000000000000
Access Rule..... Word, Double Word
Width ..... 48 bits

Bit	Bit Name	R/W	Bit Description
47..0	StationAddress	R/W	StationAddress is used to define the value which the device will compare against the Destination Address field within received Ethernet frames. Ethernet addresses are generally specified as a collection of six 8-bit hexadecimal values separated by colons as in the following example: 01:23:45:67:89:AB This example address would be written to StationAssress as the following 48-bit hexadecimal value: 0xAB8967452301

The address comparison logic within the device will compare the bits within the Destination Address field (in order, with the first received bit as bit 0, and the last received bit as bit 47) of a received Ethernet frame with the orresponding bit within StationAddress. A match is detected if each bit in the Destination Address field of the received Ethernet frame matches the corresponding bit in StationAddress.
The value in StationAddress is not inserted into the Source Address field of Ethernet frames transmitted by the device. The Source Address field for each Ethernet frame must be specified by the host system as part of the frame contents.

8.10.6.31 StatisticsMask

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset..... 0x9C
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

Bit	Bit Name	R/W	Bit Description
0	OctetRcvOk/FramesRcvdOk	R/W	OctetRcvOk/FramesRcvdOk Mask when a logic 1 indicates the OctetRcvOk and FramesRcvdOk statistic registers will not increment.
1	McstOctetRcvdOk/McstFramesRcvdOk	R/W	McstOctetRcvdOk/McstFramesRcvdOk Mask when a logic 1 indicates the McstOctetRcvdOk and McstFramesRcvdOk statistic registers will not increment.
2	BcstOctetRcvOk/BcstFramesRcvdOk	R/W	BcstOctetRcvOk/BcstFramesRcvdOk Mask when a logic 1 indicates the BcstOctetRcvOk and BcstFramesRcvdOk statistic registers will not increment.
3	RxJumboFrames	R/W	RxJumboFrames Mask when a logic 1 indicates the RxJumboFrames statistic registers will not increment.
4	TCPChecksumErrors	R/W	TCPChecksumErrors Mask when a logic 1 indicates the TCPChecksumErrors statistic registers will not increment.
5	IPCheckSumErrors	R/W	IPCheckSumErrors Mask when a logic 1 indicates the IPCheckSumErrors statistic registers will not increment.
6	UDPCheckSumErrors	R/W	UDPCheckSumErrors Mask when a logic 1 indicates the UDPCheckSumErrors statistic registers will not increment.
7	MacControlframesRcv	R/W	MacControlframesRcvd Mask when a logic 1 indicates the

Bit	Bit Name	R/W	Bit Description
	d		MacControlframesRcvd statistic registers will not increment.
8	FrameTooLongErrors	R/W	FrameTooLongErrors Mask when a logic 1 indicates the FrameTooLongErrors statistic registers will not increment.
9	InRngleLengthErrors	R/W	InRngleLengthErrors Mask when a logic 1 indicates the InRngleLengthErrors statistic registers will not increment.
10	FramesCheckSeqErrors	R/W	FramesCheckSeqErrors Mask when a logic 1 indicates the FramesCheckSeqErrors statistic registers will not increment.
11	FramesLostRxErrors	R/W	FramesLostRxErrors Mask when a logic 1 indicates the FramesLostRxErrors statistic registers will not increment.
12	OctetXmtOk/FramesXmtdOk	R/W	OctetXmtOk/FramesXmtdOk Mask when a logic 1 indicates the OctetXmtOk and FramesXmtdOk statistic registers will not increment.
13	McstOctetXmtOk/McstFramesXmtdOk	R/W	McstOctetXmtOk/McstFramesXmtdOk Mask when a logic 1 indicates the McstOctetXmtOk and McstFramesXmtdOk statistic registers will not increment.
14	BcstOctetXmtOk/BcstFramesXmtdOk	R/W	BcstOctetXmtOk/BcstFramesXmtdOk Mask when a logic 1 indicates the BcstOctetXmtOk and BcstFramesXmtdOk statistic registers will not increment.
15	FramesWDeferredXmt	R/W	FramesWDeferredXmt Mask when a logic 1 indicates the FramesWDeferredXmt statistic registers will not increment.
16	LateCollisions	R/W	LateCollisions Mask when a logic 1 indicates the LateCollisions statistic registers will not increment.
17	MultiColFrames	R/W	MultiColFrames Mask when a logic 1 indicates the MultiColFrames statistic registers will not increment.
18	SingleColFrames	R/W	SingleColFrames Mask when a logic 1 indicates the Single ColFrames statistic registers will not increment.
19	TxJumboFrames	R/W	TxJumboFrames Mask when a logic 1 indicates the TxJumboFrames statistic registers will not increment.
20	CarrierSenseErrors	R/W	CarrierSenseErrors Mask when a logic 1 indicates the CarrierSenseErrors statistic registers will not increment.
21	MacControlFramesXmtd	R/W	MacControlFramesXmtd Mask when a logic 1 indicates the MacControlFramesXmtd statistic registers will not increment.
22	FramesAbortXSColls	R/W	FramesAbortXSColls Mask when a logic 1 indicates the FramesAbortXSColls statistic registers will not increment.
23	FramesWEXDeferal	R/W	FramesWEXDeferal Mask when a logic 1 indicates the FramesWEXDeferal statistic registers will not increment.
31..24	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.32 TCPCheckSumErrors

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xC0
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	TCPCheckSumErrors	R/W	TCP Check Sum Errors is a count of received frames which contain TCP segments, which fail the TCP checksum as defined in RFC 793. TCPCheckSumErrors will wrap around to zero after reaching 0xFFFF. An UpdateStats interrupt (UpdateStats bit within the IntStatus

Bit	Bit Name	R/W	Bit Description
			register) will occur when TCPCheckSumErrors reaches a value of 0xC000. TCPCheckSumErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the TCPCheckSumErrors bit within the StatisticsMask register.

8.10.6.33 TFDListPtr

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x10
Default Value 0x0000000000000000
Access Rule..... Double Word
Width ..... 64 bits

Bit	Bit Name	R/W	Bit Description
39..0	TFDListPtr	R/W	TFD List Pointer. TFDListPtr holds the physical address within host system memory of the current TFD in the TFD list. A value of 0x0000000000000000 for TFDListPtr indicates that no more TFDs are containing Ethernet frame data to transmit are available. TFDListPtr can only specify host system memory addresses which are on 8-byte boundaries (i.e. bits 2 through 0 must be 0), therefore TFDs must be aligned on 8-byte physical address boundaries. TFDListPtr must be written directly by the host system initially to indicate the head of a newly created TFD list and is subsequently updated by the device as it processes TFDs in the TFD list. As the device finishes processing a TFD, it loads TFDListPtr with the value from the current TFD's TFDNextPtr field. If the device reads a value of 0x0000000000000000 from the current TFD's TFDNextPtr field, the transmit DMA process enters the polling state, waiting for a non-zero value to be written to current TFS's TFDNextPtr field.
63..40	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.34 TxDMABurstThresh

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x18
Default Value 0x08
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	TxDMABurstThresh	R/W	Transmit DMA Burst Threshold. TxDMABurstThresh sets the threshold by which the device determines when to assert transmit DMA bus master requests. The threshold is specified based on the amount of unoccupied space in the transmit FIFO in increments of 32 bytes. When the number of bytes in the transmit FIFO unoccupied by transmit data rises above the value specified by TxDMABurstThresh, the device may make a transmit DMA request on the PCI bus. If the number of bytes in the transmit FIFO occupied by transmit data exceeds the value in the FragLen sub field of the FragInfo field of the current TFD, device will make transmit DMA bus request regardless of the value in

Bit	Bit Name	R/W	Bit Description
			TxDMABurstThresh. The maximum value of TxDMABurstThresh is 0xFF, or 8192 bytes (256*32=8192). The minimum value of TxDMABurstThresh is 0x08, or 256 bytes, and any smaller value is interpreted as 0x08.

8.10.6.35 TxDMAPollPeriod

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x1A
Default Value 0xFF
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	TxDMAPollPeriod	R/W	Transmit DMA Poll Period. TxDMAPollPeriod determines the rate at which the current TFD in the transmit DMA Process is read for changes in the TFDNextPtr and TFC fields. TxDMAPollPeriod is specified in 320 ns increments. The maximum value is 256 (or 81.92 us). The minimum valid value is 0x01 (or 320 ns), and any smaller value is interpreted as 0x01. Since TxDMAPollPeriod cannot be set to 0x00, polling is always in effect during transmit DMA operation.

8.10.6.36 TxDMAUrgentThresh

Class..... I/O Registers, DMA
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x19
Default Value 0x04
Access Rule..... Byte
Width ..... 8 bits.

Bit	Bit Name	R/W	Bit Description
7..0	TxDMAUrgentThresh	R/W	Transmit DMA Urgent Threshold. TxDMAUrgentThresh sets the threshold by which the device determines when to assert transmit urgent DMA bus master requests. The threshold is specified based on the amount of occupied space in the transmit FIFO in increments of 32 bytes. When the number of bytes in the transmit FIFO occupied by transmit data falls below the value specified by TxDMAUrgentThresh, the device may make an urgent transmit DMA request on the PCI bus. An urgent transmit DMA request will have proirity over the receive DMA process, unless the receive DMA process is also making an urgent request. The maximum value of TxDMAUrgentThresh is 0xFF, or 8192 bytes (256*32=8192). The minimum value of TxDMAUrgentThresh is 0x04, or 128 bytes, and any smaller value is interpreted as 0x04.

8.10.6.37 TxJumboFrames

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value

Address Offset 0xF4
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	TxJumboFrames	R/W	Jumbo Frames Transmitted is a count of the number of frames transmitted successfully whose frame length (measured from the Destination Address field to the end of the Frame Check Sequence field) is greater than 1518 bytes (1522 bytes for VLAN tagged frames). TxJumboFrames will wrap around to zero after reaching 0xFFFF. An UpdateStats interrupt (UpdateStats bit within the IntStatus register) will occur when TxJumboFrames reaches a value of 0xC0000. TxJumboFrames is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the TxJumboFrames bit within the StatisticsMask register.

8.10.6.38 TxStartThresh

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x44
Default Value 0x0FFF
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
11..0	TxStartThresh	R/W	Transmit Start Threshold. TxStartThresh is used to control when frames are transmitted. Transmission of a frame begins when the number of double words (32-bit values) for the frame which have been transferred into the transmit FIFO is greater than the value specified by TxStartThresh. If the TxStartThresh is set too low, the transmit FIFO may experience underruns due to transfer rate differences between the transmit DMA process, and the Ethernet network. Use of TxStartThresh is not recommended for Gigabit Ethernet networks, except during transfer of jumbo frames. If the IPChecksumEnable, TCPChecksumEnable, or UDPChecksumEnable bits of the frame's TFC are a logic 1, the TxStartThresh value is ignored (since calculation of checksums requires the entire frame be transferred via transmit DMA prior to the start of frame transmission).
15..12	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

8.10.6.39 TxStatus

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x60
Default Value 0x00000000
Access Rule..... Byte
Width ..... 32 bits

TxStatus returns the status of frame transmission or transmission attempts. TxStatus is cleared when read.

Bit	Bit Name	R/W	Bit Description
0	TxError	R	Transmit Error. TxError indicates an error occurred during transmission of the frame indicated by the TxFrameId field of TxStatus. TxError is a logic 1 when either LateCollision, MaxCollisions, or TxUnderrun is a logic 1.
1	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
2	LateCollision	R	Late Collision. When LateCollision is a logic 1 the frame experienced a collison after the slot time (4,096 bit times). The TxEnable bit in the MACCtrl register must be set to a logic 1 to recover from this condition. The frame is kept in the transmit FIFO, so when the MAC is re-enabled the frame will be transmitted again. To prevent re-transmission of this frame, the FIFO must be cleared via the FIFO bit in the AsicCtrl register prior to re-enabling the MAC for transmission.
3	MaxCollisions	R	Maximum Collisions. When MaxCollisions is a logic 1 the frame was not successfully transmitted due to encountering 16 collisions. The TxEnable bit in the MACCtrl register must be set to a logic 1 to recover from this condition. The frame is discarded from the transmit FIFO, so the host system should resubmit the frame for transmission.
4	TxUnderrun	R	Transmit Underrun. When TxUnderrun is a logic 1 the frame experienced an underrun during the transmit process because the host was unable to supply the frame data fast enough to keep up with the network data rate. An underrun will halt the transmitter and the transmit FIFO. The TxReset bit within the AsicCtrl register and TxEnable bit within the MACCtrl register must be set to a logic 1 prior to re-starting any frame.
5	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
6	TxIndicateReqd	R	Transmit Indicate Requested. When TxIndicateReqd is a logic 1 the TxIndicate bit in the TFC field was a logic 1 when the transmitted frame's TFD was transferred via the transmit DMA process.
7	TxComplete	R	Transmit Complete. When TxComplete is a logic 1 the bits in the TxStatus register are valid and can be read by the host system. All fields within the TxStatus register are updated after transmission (either successfully or with errors) of an Ethernet frame.
15..8	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
31..16	TxFrameId	R	Transmit Frame Identifier. TxFrameId holds the value of the Ethernet frame for which the TxStatus register fields apply.

8.10.6.40 UDPCheckSumErrors

Class..... I/O Registers, Statistics
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0xC4
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	UDPChecksumErrors	R/W	UDP Check sum Errors is a count of received frames which contain UDP segments, which fail the UDP checksum as defined in RFC 768. UDPCheckSumErrors will wrap around to zero after reaching 0xFFFF. An UpdateStats interrupt (UpdateStats bit within the IntStatus

Bit	Bit Name	R/W	Bit Description
			register) will occur when UDPCheckSumErrors reaches a value of 0xC0000. UDPChecksumErrors is enabled by writing a logic 1 to the StatisticsEnable bit in the MACCtrl register, and a logic 0 to the UDPCheckSumErrors bit within the StatisticsMask register.

8.10.6.41 VLANHashTable

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x7E
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	VLANHashTable	R/W	VLAN hash Table holds a 16-bit value used for selectively receiving VLAN tagged frames. Setting the ReceiveVLANHash bit in the ReceiveMode register enables the filtering mechanism. The hash table is cleared upon reset, and must be properly set by the host. The TC9021 applies a 4-bit one's complement checksum algorithm to the 12-bit VID field of a VLAN tagged receive frame. The 4-bit checksum result is used as an addressing index into the VLAN hash table. If the VLANHashTable bit addressed by the index is a logic 1, the frame is accepted by the device and transferred to higher layers. If the VLANHashTable bit addressed by the index is a logic 0, the frame is discarded. The checksum algorithm used by the device is described below: $VID = a_{11}a_{10}a_9a_8a_7a_6a_5a_4a_3a_2a_1a_0$ $c_0b_3b_2b_1b_0 = a_{11}a_{10}a_9a_8 + a_7a_6a_5a_4$ $s_3s_2s_1s_0 = a_3a_2a_1a_0 + b_3b_2b_1b_0 + c_0$ $Checksum = s_3' s_2' s_1' s_0'$

8.10.6.42 VLANId

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x80
Default Value 0x000000000000
Access Rule..... Word
Width ..... 48 bits

Bit	Bit Name	R/W	Bit Description
11..0	VLANId0	R/W	VLAN Identification 0 specifies one, 12 bit VLAN Identifier (corresponding to the VID field of the VLAN tag portion of a receive frame) used for receive frame filtering as defined by the ReceiveMode register ReceiveVLANMatch bit. Bit 11 of VLANId0 corresponds to the most significant bit of the VID.
23..12	VLANId1	R/W	VLAN Identification 1 specifies one, 12 bit VLAN Identifier (corresponding to the VID field of the VLAN tag portion of a receive frame) used for receive frame filtering as defined by the ReceiveMode register ReceiveVLANMatch bit. Bit 23 of

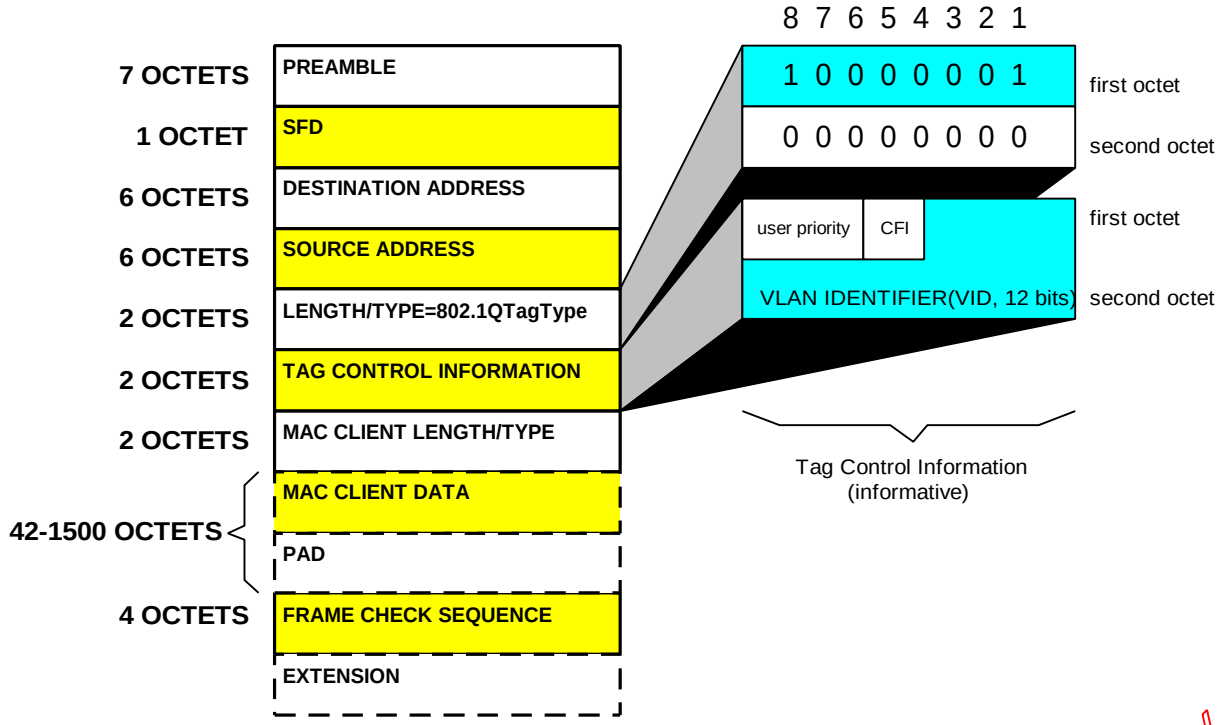
Bit	Bit Name	R/W	Bit Description
			VLANId1 corresponds to the most significant bit of the VID.
35..24	VLANId2	R/W	VLAN Identification 2 specifies one, 12 bit VLAN Identifier (corresponding to the VID field of the VLAN tag portion of a receive frame) used for receive frame filtering as defined by the ReceiveMode register ReceiveVLANMatch bit. Bit 35 of VLANId2 corresponds to the most significant bit of the VID.
47..36	VLANId3	R/W	VLAN Identification 3 specifies one, 12 bit VLAN Identifier (corresponding to the VID field of the VLAN tag portion of a receive frame) used for receive frame filtering as defined by the ReceiveMode register ReceiveVLANMatch bit. Bit 47 of VLANId3 corresponds to the most significant bit of the VID.

8.10.6.43 VLANTag

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x70
Default Value 0x81000000
Access Rule..... Double Word
Width ..... 32 bits

The VLANTag register contains the information used by the device when inserting a VLAN tag within a frame based on the state of the AutoVLANtagging bit of the MACCtrl register. The format of a VLAN tag as defined in IEEE 802.3Q is shown in Figure 10.

FIGURE 10: VLAN Tag Format from IEEE 802.3 Standard.



Bit	Bit Name	R/W	Bit Description
11..0	VID	R/W	VLAN Identifier. VID indicates the VLAN to which the Ethernet frame belongs. The VID is encoded as an unsigned binary number. A value of 0x000 indicates the Tag Header contains only

Bit	Bit Name	R/W	Bit Description
			"user_priority" information; no VLAN identifier is present in the frame. The values 0x001 and 0xFFF are reserved, all other values may be used as valid VLAN identifiers.
12	CFI	R/W	Canonical Format Indicator. When CFI is a logic 0, all MAC address information that may be present in the MAC data carried by the frame is in Canonical format. When CFI is a logic 1, the E-RIF field is present in the Tag Header, and that the NCFI bit in the RIF field determines whether MAC address information that may be present in the MAC data carried by the frame is in Canonical or Non-canonical format. See IEEE 802.3Q for more information.
15..13	UserPriority	R/W	User Priority. UserPriority indicates the priority of the Ethernet frame. Values of 0 through 7 are valid. See IEEE 802.3Q for more information.
23..16	TPID2	R/W	Tag Protocol Identifier Octet 2. TPID2 is the second octet transmitted (or received) of the QTag Prefix field within an Ethernet frame. TPID2 value must always be 0x00.
31..24	TPID1	R/W	Tag Protocol Identifier Octet 1. TPID1 is the first octet transmitted (or received) of the QTag Prefix field within an Ethernet frame. TPID1 value must always be 0x81.

8.10.6.44 WakeEvent

Class..... I/O Registers, Control and Status
I/O Base Address ..... IoBaseAddress register value
Memory Base Address . MemBaseAddress register value
Address Offset 0x51
Default Value 0x08
Access Rule..... Byte
Width ..... 8 bits
WakeEvent contains enable bits to control which types of events can generate a wake event to the host system. WakeEvent also contains status bits indicating the specific wake events which have occurred.

Bit	Bit Name	R/W	Bit Description
0	WakePktEnable	R/W	Wake Packet Enable.When WakePktEnable is a logic 1 the device generates wake events via a PCI interrupt due to reception of a Wake Packet (see section 8.4 for more details). The PmeEn bit in the PowerMgmtCtrl register must be a logic 1 in order for WakePktEnable to be recognized. WakePktEnable has no effect in power mode D0.
1	MagicPktEnable	R/W	Magic Packet Enable. When MagicPktEnable is a logic 1 the device generates wake events via a PCI interrupt due to reception of a Wake Packet (see section 8.4 for more details). The PmeEn bit in the PowerMgmtCtrl register must be a logic 1 in order for MagicPktEnable to be recognized. MagicPktEnable has no effect in power mode D0.
2	LinkEventEnable	R/W	Link Event Enable. When LinkEventEnable is a logic 1 the device generates wake events via a PCI interrupt due to a change in the PHYLNK10N SIGNAL (i.e. a change in the link status). The PmeEn bit in the PowerMgmtCtrl register must be a logic 1 in order for LinkEventEnable to be recognized. LinkEventEnable has no effect in power mode D0.
3	WakePolarity	R/W	Wake Polarity. When WakePolarity is a logic 1, the WAKE signal is asserted in the HIGH state. When WakePolarity is a logic 0, the WAKE signal is asserted in the LOW state.

Bit	Bit Name	R/W	Bit Description
4	WakePktEvent	R	Wake Packet Event. When WakePktEvent is a logic 1, a Wake Packet which meets the reception criteria set by the host system (see section 8.4 for more details) has been received. WakePktEnable must be a logic 1 in order for WakePktEvent to indicate Wake Packet reception. WakePktEvent is cleared when the WakeEvent register is read.
5	MagicPktEvent	R	Magic Packet Event. When MagicPktEvent is a logic 1, a Magic Packet which meets the reception criteria set by the host system (see section 8.4 for more details) has been received. MagicPktEnable must be a logic 1 in order for MagicPktEvent to indicate Wake Packet reception. MagicPktEvent is cleared when the WakeEvent register is read.
6	LinkEvent	R	Link Event. When LinkEvent is a logic 1, a change in the PHYLNK10N signal (i.e. a change in the link status) has occurred. LinkEventEnable must be a logic 1 in order for LinkEvent to indicate Wake Packet reception. LinkEvent is cleared when the WakeEvent register is read.
7	WakeOnLanEnable	R/W	Wake On LAN Enable. When WakeOnLanEnble is a logic 1 the device is placed in the WakeOnLan Mode (see section 8.5 for more details) regardless of the PowerMgmtCtrl register settings.

8.10.7 PCI Configuration Registers

PCI based systems use a slot-specific block of configuration registers to perform configuration of devices on the PCI bus. The configuration registers are accessed with PCI Configuration Cycles. The PCI bus supports two types of Configuration Cycles. Type 0 cycles are used to configure devices on the local PCI bus.

Type 1 cycles are used to pass a configuration request to a PCI bus at a different hierarchical level. PCI Configuration Cycles are directed at one out of eight possible PCI logical functions within a single physical PCI device. A TC9021 based PCI bus master device responds only to Type 0 Configuration Cycles, directed at function 0. Type 1 cycles, and Type 0 cycles directed at functions other than 0, are ignored by the TC9021.

Each PCI bus device is required to decode 256 bytes of configuration registers. Of these, the first 64 bytes are predefined by the PCI Specification. The remaining registers may be used as needed for PCI device-specific configuration registers. In PCI Configuration Cycles, the host system provides a slot-specific decode signal (IDSEL) which informs the PCI device that a configuration cycle is in progress. The PCI device responds by asserting DEVSELN, and decoding the specific configuration register from the address bus and the byte enable signals. See the PCI Expansion ROM specification for information on generating configuration cycles from driver software.

Table 12 shows the PCI configuration registers implemented by TC9021. All locations marked "Reserved", and all of the locations within the 256-byte configuration space (0xFF through 0x00) that are not shown in the table, are not implemented and return zero when read.

TABLE 12: TC9021 PCI Register Layout

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
Data	Reserved	PowerMgmtCtrl		54
PoweMgmtCap		NextItemPtr	CapId	50
Reserved				4C
Reserved				48
Reserved				44
Reserved				40
MaxLat	MinGnt	InterruptPin	InterruptLine	3C

BYTE 4	BYTE 3	BYTE 2	BYTE 1	ADDR OFFSET
Reserved				38
Reserved			CapPtr	34
ExpromBaseAddress				30
Subsystemld		SubsystemVendorld		2C
Reserved				28
Reserved				24
Reserved				20
Reserved				1C
Reserved				18
MemBaseAddress				14
IoBaseAddress				10
Reserved	HeaderType	LatencyTimer	CacheLineSize	0C
ClassCode			RevisionId	08
ConfigStatus		Configcommand		04
DeviceId		VendorId		00

8.10.7.1 CacheLineSize

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x0C
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	CacheLineSize	R/W	Cache Line Size. The system BIOS writes the system's cache line size into CacheLineSize. The host system uses CascheLineSize to optimize PCI bus master operation (choosing the best memory command, etc.). The value in CacheLineSize represents the number of double words in a cache. CacheLineSize values must be a power of two, from 0x04 to 0x40 (giving a range of 16 to 256 bytes). CacheLineSize values which are not a power of two, between 4 and 64 are interpreted as 0x00.

8.10.7.2 CapId

Class..... PCI Configuration Registers, Power Management
I/O Base Address ..... PCI device configuration header start
Address Offset 0x50
Default Value 0x01
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	CapId	R	Capabilities ID. CapId indicates the type of the capability data structure for the device. CapId is set to the value 0x01 to indicate a PCI Power Management structure.

8.10.7.3 CapPtr

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start

Address Offset 0x34
Default Value 0x50
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	CapPtr	R	Capabilities Pointer. CapPtr indicates the beginning of a chain of registers which describe enhanced functions. CapPtr register returns 0x50, which is the address of the first in a series of power management registers.

8.10.7.4 ClassCode

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x09
Default Value 0x020000
Access Rule..... Byte
Width ..... 24 bits

Bit	Bit Name	R/W	Bit Description
23..0	ClassCode	R	Class Code. ClassCode identifies the general function of the PCI device. A value of 0x020000 indicates an Ethernet network controller.

8.10.7.5 ConfigCommand

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x04
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits
ConfigCommand provides control over the device's ability to generate and respond to PCI cycles. When ConfigCommand is a logic 0, the device is logically disconnected from the PCI bus, except for configuration cycles.

Bit	Bit Name	R/W	Bit Description
0	IoSpace	R/W	I/O Space. When IoSpace is a logic 1 the device can respond to I/O space accesses (if the device is in the D0 power state).
1	MemorySpace	R/W	Memory Space. When MemorySpace, and the AddressDecodeEnable bit in the ExpRombaseAddress register are both a logic 1, and if the device is in the D0 power state, the device is able to decode accesses to an Expansion ROM (if present).
2	BusMaster	R/W	Bus Master. When BusMaster is a logic 1 the device is able to initiate bus master cycles (if the adapter is in the D0 power state).
3	Reserved	N/A	Reserved for future use. Write as zero ignore on read.
4	MWIEnable	R/W	Memory Write and Invalidate Enable. When MWIEnable is a logic 1 the device is permitted to use the MWI command.
5	Reserved	N/A	Reserved for future use. Write as zero ignore on read.
6	ParityErrorResponse	R/W	Parity Error Response. When ParityErrorResponse is a logic 1 the device responds to parity errors as defined within the PCI specification. When ParityErrorResponse is a logic 0, the device ignores parity errors
7	Reserved	N/A	Reserved for future use. Write as zero ignore on read.

Bit	Bit Name	R/W	Bit Description
8	SERREnable	R/W	System Error Enable. When SERREnable is a logic 1, the SERRN signal is allowed to transmition as appropriate. When SERREnable is a logic 0, the SERRN signal is a continuous logic 0.
15..9	Reserved	N/A	Reserved for future use. Write as zero ignore on read.

8.10.7.6 ConfigStatus

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset..... 0x06
Default Value 0x0230
Access Rule..... Word
Width ..... 16 bits

ConfigStatus is used to record status information for PCI bus events. Read/write bits within ConfigStatus can only be set to a logic 0, not to a logic 1. Bits are set to a logic 0 by writing a logic 1 to the appropriate bit.

Bit	Bit Name	R/W	Bit Description
3..0	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
4	Capabilities	R	Capabilities. Capabilities is a logic 1 to indicate a set of extended capabilities registers exists for the device. The CapPtr register indicates the first address location of the extended capabilities register set.
5	66MHzCapable	R	66MHz Capable. When 66MhzCapable is a logic 1 operation of the device PCI bus interface at 66MHz is supported.
6	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
7	FastBackToBack	R	Fast Back to Back. When FastBackToBack is a logic 1 the device when operating as a Target, supports fast back-to-back transactions as defined by the criteria in the section 3.4.2 of the PCI specification.
8	DataParityReported	R	Data Parity Reported. When DataParityReported is a logic 1, the device when operating as a Master, has detected the PERRN signal asserted, and the ParityErrorResponse bit in the ConfigCommand register as a logic 1.
10..9	DevselTiming	R	Device Select Timing. DevselTiming is used to encode the slowest time with which the device asserts the DEVSELN signal. A value of 0x1 for DevselTiming indicates support for “medium” speed DEVSELN assertion.
11	SignaledTargetAbort	R	Signaled Target Abort. The device sets SignaledTargetAbort to a logic 1 when the device terminates a bus transaction with target-abort.
12	ReceivedTargetAbort	R	Received Target Abort. The device sets ReceivedTargetAbort to a logic 1 when, operating as a bus master, a bus transaction is terminated with target-abort.
13	ReceivedMasterAbort	R	Received Master Abort. The device sets ReceivedMasterAbort to a logic 1 when, operating as a bus master, a bus transaction is terminated with master-abort.
14	SignaledSystemError	R	Signaled System Error. When SignaledSystemError is a logic 1, the device asserts the SERRN signal.
15	DetectedParityError	R	Detected Parity Error. When DetectedParityError is a logic 1 the device has detected a parity error, regardless of whether parity error handling is enabled.

8.10.7.7 Data

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset..... 0x57
Default Value 0x0000
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	Data	R	Data reports power consumption and dissipation of the TC9021 at worst case conditions. To properly interpret the value read from Data, it must be scaled by the factor indicated in the Data_Scale field of the PowerMgmtCtrl register. The value of Data depends on the value of the Data_Select field of the PowerMgmtCtrl register. **Data_Select** **Data** 0x0 40*Data_Scale Watts D0 Power Consumption 0x1 40*Data_Scale Watts D1 Power Consumption 0x2 40*Data_Scale Watts D2 Power Consumption 0x3 40*Data_Scale Watts D3 Power Consumption 0x4 40*Data_Scale Watts D4 Power Consumption 0x5 40*Data_Scale Watts D5 Power Consumption 0x6 40*Data_Scale Watts D6 Power Consumption 0x7 40*Data_Scale Watts D7 Power Consumption 0x8 through 0xF 0x00 Reserved.

8.10.7.8 DeviceId

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x02
Access Rule..... Word
Default Value 0x2020
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description

Bit	Bit Name	R/W	Bit Description
15..0	DeviceId	R/W	Device ID. DeviceId contains the 16-bit device identifier for the TC9021, set to 0x9021

8.10.7.9 ExpRomBaseAddress

Class..... PCI Configuration Registers, Configuration
I/O Base Address ..... PCI device configuration header start
Address Offset 0x30
Default Value 0x00000000
Access Rule..... Double Word
Width 0x32
ExpRomBaseAddress defines the base address for an Expansion ROM which may be interfaced to the device.

Bit	Bit Name	R/W	Bit Description
0	AddressdecodeEnable	R/W	Address Decode Enable. When addressDecodeEnable is a logic 0 accesses to an Expansion ROM are disabled. When AddressDecodeEnable is a logic 1 and the MemorySpace bit in the ConfigCommand register is also a logic 1, accesses to an Expansion ROM are enabled.
14..1	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
31..15	RomBaseAddress	R/W	ROM Base Address. RomBaseAddress contains the expansion ROM base address, or the upper 16 bits (or 15 bits, depending on the state of the ExpRomSize bit in the AsicCtrl register) of the Expansion ROM address range. If the ExpRomsize bit in the AsicCtrl register is a logic 0, all 16 bits of RomBaseAddress are valid. If the ExpRomSize bit in the AsicCtrl register is a logic 1, bits 31 through 16 of RombaseAddress are valid, with bit 15 ignored (set to a logic 0) during write operations.

8.10.7.10 HeaderType

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x0E
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	HeaderType	R	Header Type. HeaderType is set to 0x00 identifying the TC9021 as a single-function PCI device and specifying the configuration register layout.

8.10.7.11 InterruptLine

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x3C
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	InterruptLine	R/W	Interrupt Line. InterruptLine specifies the interrupt level used by

Bit	Bit Name	R/W	Bit Description
			the device. By setting InterruptLine the host sysem may configure the appropriate interrupt vector for its Interrupt Service Routine. For 80x86 processor based host systems, InterruptLine corresponds to the IRQ number (0x00 through 0x0F), with the value 0xFF corresponding to disabled interrupts.

8.10.7.12 InterruptPin

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x3D
Default Value 0x01
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	InterruptPin	R	Interrupt Pin. InterruptPin indicates which PCI interrupt signal the device will utilize. The TC9021 always utilizes the INTAN interrupt signal, corresponding to an InterruptPin value of 0x01.

8.10.7.13 IoBaseAddress

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x10
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits

The host uses IoBaseAddress to define the I/O base address for the device. PCI system requires that I/O base addresses be set as if the host system used 32-bit I/O addressing. The upper 24 bits of IoBaseAddress are accessible, indicating that the TC9021 requires 256 bytes in the host system I/O address space.

Bit	Bit Name	R/W	Bit Description
0	IoBaseAddrInd	R/W	I/O Base Address Indicator. When IoBaseAddrInd is a logic 1, IoBaseAddress contains the valid I/O base address for the device.
7..1	Reseved	N/A	Reserved for future use. Write as zero, ignore on read.
31..8	IoBaseAddress	R/W	I/O Base Address. IoBaseAddress contains the 24 bit I/O base address value. With 24 bits, the TC9021 uses 256 bytes of I/O address space.

8.10.7.14 LatencyTimer

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x0D
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
2..0	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
7..3	LatencyTimer	R/W	Latency Timer. LatencyTimer indicates, in increments of 8 bus clocks, the length of time which the device may hold the PCI bus in the presence of other bus requestors. Whenever the device asserts the FRAMEN signal, the latency timer is started. When the

Bit	Bit Name	R/W	Bit Description
			latency timer count expires, the device must relinquish the bus as soon as its GNTN signal has been deasserted.

8.10.7.15 MaxLat

Class..... PCI Configuration Registers, Configuration
I/O Base Address ..... PCI device configuration header start
Address Offset 0x3F
Default Value 0x05
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	MaxLat	R	Maximum Latency. MaxLat specifies, in 250 ns increments, how often the device requires bus access while operating as a bus master. The value for MaxLat is loaded from the CongigParm field within an EEPROM during auto initialization of the device.

8.10.7.16 MemBaseAddress

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x34
Default Value 0x00000000
Access Rule..... Double Word
Width ..... 32 bits
MemBaseAddress can be disabled via loading of the ConfigParm field from an EEPROM during auto-initialization of the TC9021.

Bit	Bit Name	R/W	Bit Description
0	MemBaseAddrInd	R/W	Memory Base Address Indicator. When MemBaseAddrInd is a Logic 1, MemBaseAddress contains the valid memory base address.
2..1	MemMapType		Memory Map Type. MemMapType defines how the host system maps the TC9021's registers within the host system memory space. Bit 2 of MemMapType is always a logic 0, while bit 1 is loaded from the Lower1Meg bit of the ConfigParm field within an EEPROM during auto initialization of the device. **Bit 1** **Bit 0** **Ethernet Frame TCI Priority Field Bit** 0 0 Anywhere within a 32-bit address space 0 1 Lower 1 megabyte of 32-bit address apace 1 X Undefined
8..3	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.

Bit	Bit Name	R/W	Bit Description
31..9	MemBaseAddress	R/W	Memory Base Address. MemBaseAddress contains the 23 bit memory base address value. With 23 bits, the TC9021 uses 512 bytes of I/O apace.

8.10.7.17 MinGnt

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x3E
Default Value 0x0A
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	MinGnt	R	Minimum grant Time. MinGnt specifies, in 250 ns increments, how long a burst period the device requires when operating as a bus master. The value for MinGnt is loaded from the ConfigParm field within an EEPROM during auto initialization of the TC9021.

8.10.7.18 NextItemPtr

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x51
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	NextItemPtr	R	Next Item Pointer. NextItemPtr indicates the next capability data structure in the capabilities list. NextItemPtr is set to the value 0x00 to indicate there are no further data structures.

8.10.7.19 PowerMgmtCap

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x52
Default Value 0x7601
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
2..0	Version	R	Version. Version is set to 0x2, indicating PCI Bus Power Management Specification Revision 1.1.
8..3	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
9	D1Support	R	D1 Power State Support. When D1Support is a logic 1, the device supports the D1 power state (see section 8.4). D1Support is loaded from the ConfigParm field of an EEPROM during auto initialization of the device.
10	D2Support	R	D2 Power State Support. When D2Support is a logic 1, the device supports the D2 power state (see section 8.4). D2Support is loaded from the ConfigParm field of an EEPROM during auto initialization of the device.
15..11	Pmesupport	R	Power management EventSupport. PmeSupport indicates the power states from which the device is able to generate a power

Bit	Bit Name	R/W	Bit Description
			management event by asserting the WAKE signal. Each bit corresponds to a power state. A logic 1 in a particular bit position indicates that event can be generated from the indicated power state. **Bit 15** **Bit 14** **Bit 13** **Bit 12** **Bit 11** **Power Management Event May Be Generated From State** X X X X 1 D0 X X X 1 X D1 X X 1 X X D2 X 1 X X X D3Hot 1 X X X X D3Cold PmeSupport bits 14 and 11 are always set to a logic 1 while bits 12, 13 , and 15 are loaded from the ConfigParm field of an EEPROM during auto initialization of the device.

8.10.7.20 PowerMgmtCtrl

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x54
Default Value 0x0000

Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
1..0	PowerState	R/W	Power State. PowerState Indicates the current power state of the device. If PowerState is set to a value other than 0x0, the device will not respond to PCI I/O or memory cycles, nor will the device be able to generate PCI bus master cysles. **Bit 1** **Bit 0** **Power State** 0 0 D0 0 1 D1 1 0 D2 1 1 D3
7..2	Reserved	N/A	Reserved for future use. Write as zero, ignore on read.
8	PmeEn	R/W	Power Management Event Enable. When PmeEn is a logic 1, the device is allowed to report wake events on the WAKE signal. The criteria for generating wake events is defined by the WakeEvent register. PmeEn is loaded from the ConfigParm field of an EEPROM during auto initialization of the device.
12..9	Data_Select	R/W	Data Select is used ot select which data is to be reported through the Data register and Data_Scale field.
14..13	Data_Scale	R	Data Scale Only indicates the scaling factor to be used when interpreting the value of the Data register. The interpretation of the scale values is defined as follows: **Data_Scale** **Scale Factor** 0x0 Unknown 0x1 0.1 0x2 0.01 0x3 0.001

Bit	Bit Name	R/W	Bit Description
15	PmeStatus	R/W	Power Management Event Status. When PmeStatus is a logic 1 a wake event has occurred. PmeStatus may be a logic 1 regardless of the value of PmeEn. Writing a logic 1 to PmeStatus will set PmeStatus to a logic 0. Writing a logic 0 to PmeStatus has no effect.

8.10.7.21 RevisionId

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x08
Default Value 0x00
Access Rule..... Byte
Width ..... 8 bits

Bit	Bit Name	R/W	Bit Description
7..0	RevisionId	R	Revision ID. RevisionId contains a revision code for the TC9021. The first TC9021 will return the value 0x00 for ReviesionId. For each revision of the device, RevisionId will be incremented.

8.10.7.22 SubsystemId

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x2E
Default Value 0x0000
Access Rule..... Byte
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	SubsystemId	R	Subsystem ID. SubsystemId contains the value loaded from the ConfigParm field within an EEPROM during auto initialization of the device.

8.10.7.23 SubsystemVendorId

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x2C
Default Value 0x0000
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	SubsystemVendorId	R	Subsystem Vendor ID. SubsystemVendorId contains the value loaded form the ConfigParm field within an EEPROM during auto initialization of the device

8.10.7.24 VendorId

Class..... PCI Configuration Registers
I/O Base Address ..... PCI device configuration header start
Address Offset 0x00
Default Value 0x143D
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..0	VendorId	R	Vendor ID. VendorId contains the unique 16-bit manufacturer's ID as allocated by the PCI Special Group. Tamarack Microelectronics Inc. manufacturer ID is 0x143D.

8.10.8 EEPROM Fields

Table 13 summarizes the layout of the data stored in an EEPROM connected to the device. Most defined EEPROM fields are read from the EEPROM and loaded into unique register bit positions within the device during auto initialization (see 8.10.6.1).
In Table 13, all locations marked "Unused" and all locations not shown are not utilized by the device.

TABLE 13: TC9021 EEPROM Field Layout

16-bit Word	ADDR OFFSET
StationAddress	12
StationAddress	11
StationAddress	10
Unused	F
Unused	E
Unused	D
Unused	C
Unused	B
Unused	A
Unused	9
Unused	8
Unused	7
Unused	6
Unused	5
Unused	4
SubsystemId	3
SubsystemVendorId	2
AsicCtrl	1
ConfigParm	0

8.10.8.1 AsicCtrl

Class..... EEPROM Fields
I/O Base Address ..... 0x00, accessed via the EepromCtrl register
Address Offset 0x01
Access Rule..... Word
Width ..... 16 bits
ASIC Control supplies the value for several bits of the AsicCtrl register and the WakeEvent register.

Bit	Bit Name	Bit Description
0	Reserved	Reserved for future use. Write as zero, ignore on read.
1	ExpRomSize	Expansion ROM Size. ExpRomSize corresponds to the ExpRomSize bit in the AsicCtrl register.
2	Reserved	Reserved for future use. Write as zero

Bit	Bit Name	Bit Description
3	Reserved	Reserved for future use. Write as zero
4	Reserved	Reserved for future use. Write as zero
5	PhySpeed100	Physical Layer Device Speed 100. PhySpeed100 corresponds to the PhySpeed100 bit in the AsicCtrl register.
6	PhySpeed1000	Physical Layer Device Speed 1000. PhySpeed1000 corresponds to the PhySpeed1000 bit AsicCtrl register.
7	PhyMedia	Physical Layer Device Media. PhyMedia corresponds to the PhyMedia bit in the AsicCtrl register.
14..8	Reserved	Reserved for future use. Write as zero, ignore on read.
15	WakeOnLanPolarity	Wake On LAN Polarity. WakeOnLanPolarity corresponds to the WakeOnLanEnable bit in the WakeEvent register.

8.10.8.2 ConfigParm

Class..... EEPROM Fields
I/O Base Address ..... 0x00, accessed via the EepromCtrl register
Address Offset 0x00
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	Bit Description
0	FastBackToBack	Fast Back to Back. FastBackToBack corresponds to the FastBackToBack bit of the ConfigStatus register.
1	Lower1Meg	Lower 1 Megabyte. Lowe1Meg corresponds to bit 1 of the MemMapType field in th MemBaseAddress register.
2	DisableMemBase	Disable Memory Base Address Register. DisableMemBase does not correspond directly to any register accessible by the host system. If DisableMemBase is a logic 1 during auto initialization of the device, the MemBaseAddress register will be disabled. When disabled, the value returned when the MemBaseAddress register is read is undefined.
3	D3ColdPme	D3 Cold Power Management Event. D3ColdPme corresponds to bit 15 of the PmeSupport field within the PowerMgmtCap register.
4	D1Support	D1 Power State Support. D1Support corresponds to the D1Support bit of the PowerMgmtCap register, and bit 12 of the PmeSupport field within the PowerMgmtCap rgister.
5	D2Support	D2 Power State Support. D2Support corresponds to the D2Support bit of the PowerMgmtCap register, and bit 13 of the PmeSupport field within the Power MgmtCap register.
6	PmeEn	Power Management Event Enable. PmeEn corresponds to the PmeEn bit in the PowerMgmtCtrl register.
10..7	MinGnt	Minimum Grant. MinGnt corresponds to bits 4 through 1 of the MinGnt register.
15..11	MaxLat	Maximum Latency. MaxLat corresponds to bits 5 through 1 of the MaxLat register.

8.10.8.3 StationAddress

Class..... EEPROM Fields
I/O Base Address ..... 0x00, accessed via the EepromCtrl register
Address Offset 0x10
Access Rule..... Byte
Width ..... 48 bits

Bit	Bit Name	Bit Description
47..0	StationAddress	Station Address. StationAddress corresponds to the StationAddress register.

8.10.8.4 SubsystemId

Class..... EEPROM Fields
I/O Base Address ..... 0x00, accessed via the EepromCtrl register
Address Offset 0x03
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	Bit Description
15..0	SubsystemId	Subsystem ID. SubsystemId corresponds to the SubsystemId register.

8.10.8.5 SubsystemVendorId

Class..... EEPROM Fields
I/O Base Address ..... 0x00, accessed via the EepromCtrl register
Address Offset 0x02
Access Rule..... Word
Width ..... 16 bits

Bit	Bit Name	Bit Description
15..0	SubsystemVendorId	Subsystem Vendor ID. SubsystemVendorId corresponds to the SubsystemVendorId register.

8.10.9 PCS Management Registers

The TC9021 implementation of the IEEE 1000BASE-X Physical Coding Sublayer (or PCS) includes several management registers, defined in the IEEE 802.3 standard clause 37.2.5.1. These registers can only be accessed if the device is in TBI mode (see the GMII signal definition). The PCS management registers are similar to registers which would be present in external PHY devices incorporating a 1000BASE-X PCS implementation. The PCS management registers are accessed similarly to external PHY device registers using the TC9021 PhyCtrl register MgmtClk, MgmtData, and MgmtDir bits (see IEEE 802.3 1998 Edition for details on accessing management registers). When accessing the PCS management registers within the device, the PHY Address for all register accesses is 0x01. Table 14 shows a layout of the registers implemented in the TC9021 1000BASE-X PCS implementation.

TABLE 14: TC9021 1000BASE-X PCS Management Registers

16-bit Word	ADDR OFFSET
ExtendedStatus	F
Unused	E
Unused	D
Unused	C
Unused	B
Unused	A
Unused	9
LinkPartnerNextPage	8
NextPage	7
Expansion	6
LinkPartnerBasePage	5
Advertisement	4
Unused	3

Unused	2
Status	1
Control	0

8.10.9.1 Advertisement

Class..... PCS Management
PHY Address 0x01
Register 0x04
Default Value 0x01E0
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15	Next Page	R/W	1=indicates additional Next Pages follow 0=indicates last page
14	Reserved	R	Reserved for future use. Write as zero, ignore on read.
13..12	Remote Fault	R/W	**Bit 13** **Bit 12** **Remote Fault** 0 0 No error, link OK (default) 1 0 Offline 0 1 Link failure 1 1 Auto-negotiation failure
11..9	Reserved	R	Reserved for future use. Write as zero, ignore on read.
8..7	Pause	R/W	**Bit 8** **Bit 7** **Pause** 0 0 No PAUSE 1 0 Asymmetric PAUSE toward link partner 0 1 Symmetric PAUSE

Bit	Bit Name	R/W	Bit Description
			1 1 Both Symmetric PAUSE and Asymmetric PAUSE toward local device
6	Half Duplex	R/W	1=indicates support for half duplex 0=indicates no support for half duplex
5	Full Duplex	R/W	1=indicates support for full duplex 0=indicates no support for full duplex
4..0	Reserved	R	Reserved for future use. Write as zero, ignore on read.

8.10.9.2 Control

Class..... PCS Management
PHY Address..... 0x01
Register 0x00
Default Value 0x1140
Width ..... 16 bits

The TC9021 PCS Management Control register differs from the Control Register definition in the IEEE 802.3 standard as follows:

Bit 13 is read only since the device only implements 1000 Mbp/s operation.

Bit 11 is read only since the device does not implement separate power down of the PCS functionality.

Bit 10 is read only since the device does not implement GMII electrical isolation.

Bit 6 is read only since the device only implements 1000 Mbp/s operation.

Bit	Bit Name	R/W	Bit Description
15	Reset	R/W	1=PHY Reset (reset the PCS implementation within TC9021 0=normal operation
14	Loopback	R/W	1=enable loopback mode (asserts the MDC/EWRAP signal HIGH to indicate to the PHY device that transmit data should be wrapped to the receive interface). 0=disable loopback mode
13	SpeedSelection(LSB)	R	0=combined with bit 6 (bit 6=1) indicates 1000 Mb/s operation only.
12	Auto-Negotiation Enable	R/W	1=Enable Auto-Negotiation Process 0=Disable auto-Negotiation Process
11	Power Down	R	0=normal operation
10	Isolate	R	0=normal operation
9	Restart Auto-Negotiation	R/W	1=Restart Auto-Negotiation Process 0=normal operation
8	Duplex Mode	R/W	1=Full Duplex 0=Half Duplex
7	Collision Test	R/W	1=enable COL signal test 0=disable COL signal test
6	Speed Selection (MSB)	R	1=combined with bit 13 (bit 13=0) indicates 1000 Mb/s operation only.
5..0	Reserved	R	Reserved for future use. Write as zero, ignore on read.

8.10.9.3 Expansion

Class..... PCS Management
PHY Address 0x01
Register 0x06

Default Value 0x0004
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15..3	Reserved	R	Reserved for future use. Write as zero, ignore on read.
2	Next Page Able	R	1=indicates next page able 0=indicates not next page able
1	Page Received	R	1=indicates a new page has been received 0=indicates a new page has not yet been received
0	Reserved	R	Reserved for future use. Write as zero, ignore on read.

8.10.9.4 ExtendedStatus

Class..... PCS Management
PHY Address..... 0x01
Register 0x0F
Default Value 0xC000
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15	1000BASE-X Full Duplex	R	1=PHY able to perform full duplex 1000BASE-X 0=PHY not able to perform full duplex 1000ABSE-X
14	1000BASE-X Half Duplex	R	1=PHY able to perform half duplex 1000BASE-X 0=PHY not able to perform half duplex 1000ABSE-X
13	1000BASE-T Full Duplex	R	1=PHY able to perform full duplex 1000BASE-T 0=PHY not able to perform full duplex 1000ABSE-T
12	1000BASE-T Half Duplex	R	1=PHY able to perform half duplex 1000BASE-T 0=PHY not able to perform half duplex 1000ABSE-T
11..0	Reserved	R	Reserved for future use. Write as zero, ignore on read.

8.10.9.5 LinkPartnerBasePage

Class..... PCS Management
PHY Address 0x01
Register 0x05
Default Value 0x0000
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15	Next Page	R	1=indicates additional Next Pages follow 0=indicates last page
14	Acknowledge	R	1=indicates received link partner's code word 0=indicates link partner's code word not yet received
13..12	Remote Fault	R	**Bit 13** **Bit 12** **Remote Fault** 0 0 No error, link OK (default) 1 0 Offline

Bit	Bit Name	R/W	Bit Description
			0 1 Link failure 1 1 Auto-negotiation failure
11..9	Remote Fault	R	Reserved for future use. Write as zero, ignore on read.
8..7	Pause	R	**Bit 8** **Bit 7** **Pause** 0 0 No PAUSE 1 0 Asymmetric PAUSE toward link partner 0 1 Symmetric PAUSE 1 1 Both Symmetric PAUSE and Asymmetric PAUSE toward local device
6	Half Duplex	R	1=indicates link partner supports half duplex 0=indicates link partner does not support half duplex
5	Full Duplex	R	1=indicates link partner supports full duplex 0=indicates link partner does not support full duplex
4..0	Reserved	R	Reserved for future use. Write as zero, ignore on read.

8.10.9.6 LinkPartnerNextPage

Class..... PCS Management
PHY Address 0x01
Register 0x08
Default Value 0x0000
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15	Next Page	R	1=indicates additional Next Pages follow 0=indicates last page
14	Acknowledge	R	1=indicates received link partner's code word 0=indicates link partner's code word not yet received
13	Message Page	R	1=indicates a Message page 0=indicates an Unformatted Page
12	Acknowledge 2	R	1=indicates able to comply with message

Bit	Bit Name	R/W	Bit Description
			0=indicates not able to comply with message
11	Toggle	R	1=indicates previous value of toggle bit in code word=0 0= indicates previous value of toggle bit in code word=1
10..0	Message/Unformatted Code Field	R	11 bit message code or unformatted code.

8.10.9.7 NextPage

Class..... PCS Management
PHY Address 0x01
Register 0x07
Default Value 0x2001
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15	Next Page	R/W	1=indicates additional Next Pages follow 0=indicates last page
14	Reserved	R	Reserved for future use. Write as zero, ignore on read.
13	Message Page	R/W	1=indicates a Message Page 0=indicates an Unformatted Page
12	Acknowledge 2	R/W	1=indicates able to comply with message 0=indicates not able to comply with message
11	Toggle	R	1=indicates previous value of toggle bit in code word=0 0=indicates previous value of toggle bit in code word=1
10..0	Message/Unformatted Code Field	R/W	11 bit message code or unformatted code.

8.10.9.8 Status

Class..... PCS Management
PHY Address..... 0x01
Register 0x01
Default Value 0x0109
Width ..... 16 bits

Bit	Bit Name	R/W	Bit Description
15	100BASE-T4	R	0=Not able to perform 100BASE-T4
14	100BASE-X Full Duplex	R	0=Not able to perform 100BASE-X Full Duplex
13	100BASE-X Half Duplex	R	0=Not able to perform 100BASE-X Half Duplex
12	10 Mb/s Full Duplex	R	0=Not able to perform 10 Mb/s Full Duplex
11	10 Mb/s Half Duplex	R	0=Not able to perform 10 Mb/s Half Duplex
10	100BASE-T2 Full Duplex	R	0=Not able to perform 100BASE-T2 Full Duplex
9	100BASE-T2 Half Duplex	R	0=Not able to perform 100BASE-T2 Half Duplex
8	Extended Status	R	1=Extended status information in Register 15
7	Reserved	R	Reserved for future use. Write as zero, ignore on read.
6	MF Preamble Suppression	R	0=will not accept management frames with preamble suppressed
5	Auto-Negotiation Complete	R	1=Auto-Negotiation process completed 0=Auto-Negotiation process not completed
4	Remote Fault	R	1=remote fault condition detected

Bit	Bit Name	R/W	Bit Description
			0=no remote fault condition detected
3	Auto-Negotiation Ability	R	1=able to perform Auto-Negotiation 0=not able to perform Auto-Negotiation
2	Link Status	R	1=link is up 0=link is down
1	Jabber Detect	R	0=no jabber condition detected
0	Extended Capability	R	1=extended register capabilities

9 Absolute Maximum Ratings

Storage Temperature.....-65ºC to +150ºC
Ambient Temperature .....-65ºC to +70ºC
Supply Voltage.....-0.3V to +3.6V
Environmental stresses above those listed in Absolute Maximum Ratings may cause permanent damage resulting in device failure. Functionality at or above the limits listed below is not guaranteed. Exposure to the environmental stress at the levels listed below for extended periods may adversely affect device reliability.

10 Operating Ranges

Commercial Devices
Temperature (T_A) ..... 0ºC to +70ºC
Supply Voltages (V_{CCH}) ..... +3.3V ±10%
Supply Voltages (V_{CCL}) ..... +2.5V ±5%
Input voltages .....5V tolerant I/O
Operating ranges define the limits of guaranteed device functionality.

11 DC Characteristics

DC characteristics are defined over commercial operating ranges unless specified otherwise.

TABLE 15: DC Characteristics.

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{CCH}	3.3V power supply voltage		3.0		3.6	V
I_{CCH}	3.3V power supply current			TBD		mA
V_{CCL}	2.5V power supply voltage		2.37		2.63	V
I_{CCL}	2.5V power supply current			TBD		mA
TTL I/O						
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{IN}	Input leakage current	$V_{IN}=V_{CC}/GND$	-10		10	µA
V_{OH}	Output high voltage	I_{OH}=-2mA	2.4			V
V_{OL}	TTL Output low voltage	I_{OL}=4mA			0.4	V
V_{OL}	PCI Output low voltage	I_{OL}=3mA			0.55	V
I_{OTS}	Output tri-state leakage				10	µA

12 Switching Characteristics

TABLE 16: Switching Characteristics.

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
66 MHz PCI Interface						
T_{rc}	RSTN cycle		300			ns
T_{rr}	Rising Edge or RSTN to chip recovery		1			µs
T_{cc}	PCICLK cycle		15			ns
T_{ch}	PCICLK high		6			ns
T_{cl}	PCICLK low		6			ns
T_{rv}	PCICLK rise to bused signal valid		2		6	ns
T_{rvp}	PCICLK rise to REQN, GNTN valid		2		6	ns
T_{rzo}	PCICLK rise to signal on		2			ns
T_{roz}	PCICLK rise to signal off				14	ns
T_{su}	bused signal setup wrt PCICLK rise		3			ns
T_{sup1}	GNTN setup wrt PCICLK rise		5			ns
T_{sup2}	REQN setup wrt PCICLK rise		5			ns
T_{hd}	signal hold wrt PCICLK rise		0			ns
T_{rstoff}	RSTN low to output signal float				40	ns
33MHz PCI Interface						
T_{rc}	RSTN cycle		300			ns
T_{rr}	Rising edge or RSTN to chip recovery		1			µs
T_{cc}	PCICLK cycle		30			ns
T_{ch}	PCICLK high		11			ns
T_{cl}	PCICLK lwo		11			ns
T_{rv}	PCICLK rise to bused signal valid		2		11	ns
T_{rvp}	PCICLK rise to REQN, GNTN valid		2		12	ns
T_{rzo}	PCICLK rise to signal on		2			ns
T_{roz}	PCICLK rise to signal off				28	ns
T_{su}	bused signal setup wrt PCICLK rise		7			ns
T_{sup1}	GNTN setup wrt PCICLK rise		10			ns
T_{sup2}	REQN setup wrt PCICLK rise		12			ns
T_{hd}	signal hold wrt PCICLK rise		0			ns
T_{rstoff}	RSTN low to output signal float				40	ns
Expansion Rom Interface - Read						
T_{adv}	ED valid from EA stable		0		150	ns
T_{odv}	ED valid from EOEN low		0		70	ns
T_{dvz}	ED tri-stated from EOEN high		0		40	ns
Expansion Rom Interface – Load						
T_{as}/T_{os}	EA, EOEN setup wrt EWEN fall		0			ns
T_{ah}	EA hold wrt EWEN fall		50			ns
T_{ds}	ED setup wrt EWEN rise		35			ns
T_{dh}/T_{oh}	ED, EOEN hold wrt EWEN fall		0			ns
T_{wh}	EWEN write cycle high		100		-	ns

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
T_{wl}	EWEN write cycle low		90		-	ns
EEPROM Interface						
T_{skc}	EESK cycle		1µs		-	ns
T_{skh}	EESK high		250		-	ns
T_{skl}	EESK low		250		-	ns
T_{cs}	EECS low		250		-	ns
T_{pd}	EEDI valid wrt EESK rise		100		-	ns
T_{csk}	EECS setup wrt EESK rise		50		-	ns
T_{csh}	EECS hold wrt EESK fall		0		-	ns
T_{dos}	EEDO setup wrt EESK rise		70		500	ns
T_{doh}	EEDO hold wrt EESK rise		-		500	ns
MII Interface (10/100) – Transmit						
T_{cc}	TXCLK cycle	T=1 when 100Mb/s; 10 when 10Mb/s		40T		ns
T_{ch}	TXCLK high		14T		26T	ns
T_{cl}	TXCLK low		14T		26T	ns
T_{rv}	TXCLK rise to TXD, TXEN valid				20	ns
T_{rh}	TXD, TXEN hold after TXCLK rise		5			ns
MII Interface (10/100) – Receive						
T_{cc}	RXCLK cycle	T=1 when 100Mb/s; 10 when 10Mb/s	-	40T		ns
T_{ch}	RXCLK high		14T		26T	ns
T_{cl}	RXCLK low		14T		26T	ns
T_{su}	RXD, RXER, RXDV setup wrt RXCLK rise		10		20	ns
T_{hd}	RXD, RXER, RXDV hold wrt RXCLK rise		5			ns
GMII Interface (1000) – Transmit						
T_{cc}	GTXCLK cycle			8		ns
T_{ch}	GTXCLK high		7.5		8.5	ns
T_{cl}	GTXCLK low		7.5		8.5	ns
T_{rv}	GTXCLK rise to TXD, TXEN valid				20	ns
T_{rh}	TXD, TXEN hold after GTXCLK rise		5			ns
GMII/TBI Interface (1000) – Receive						
T_{cc}	RXCLK0 cycle		-	8		ns
T_{ch}	RXCLK0 high		7.5		8.5	ns
T_{cl}	RXCLK0 low		7.5		8.5	ns
T_{su}	RXD, RXER, RXDV setup wrt RXCLK0 rise		10		20	ns
T_{hd}	RXD, RXER, RXDV hold wrt RXCLK0 rise		5			ns
MII Interface – Management						
T_{cc}	MDC cycle		400	-	-	ns
T_{ch}	MDC high		160		-	ns

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
T_{cl}	MDC low		160		-	ns
T_{su}	MDIO setup wrt MDC rise		10		-	ns
T_{hd}	MDIO hold wrt MDC rise		10		-	ns
T_{rv}	MDC rise to MDIO valid		-		20	ns
MISC Interface						
T_{cc}	CLK125 cycle			8.0		ns
T_{ch}	CLK125 high			4.0		ns
T_{cl}	CLK125 low			4.0		ns

FIGURE 11: PCI Switching Characteristics

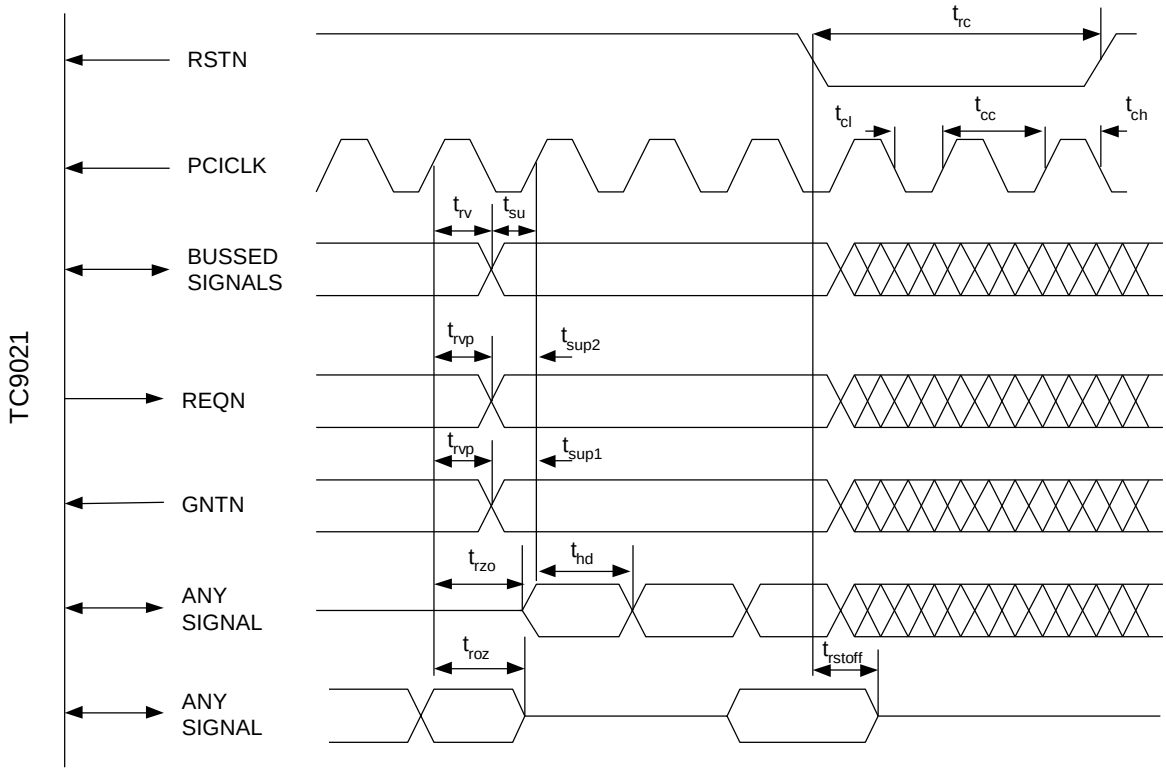


FIGURE 12: Expansion ROM Switching Characteristics.

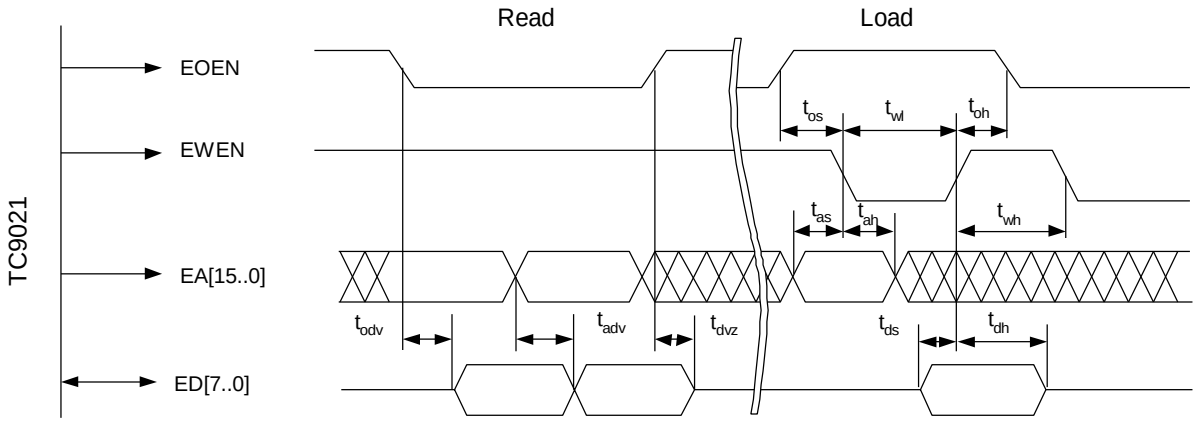


FIGURE 13: EEPROM Switching Characteristics

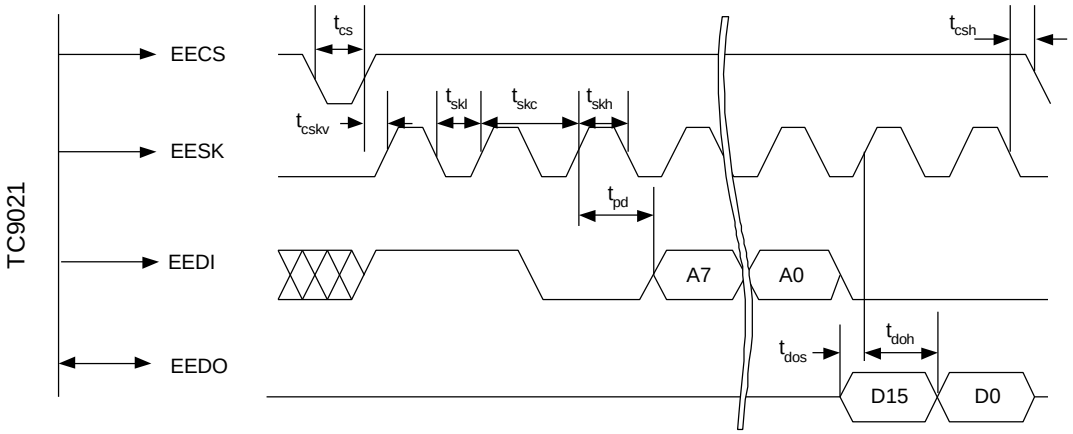
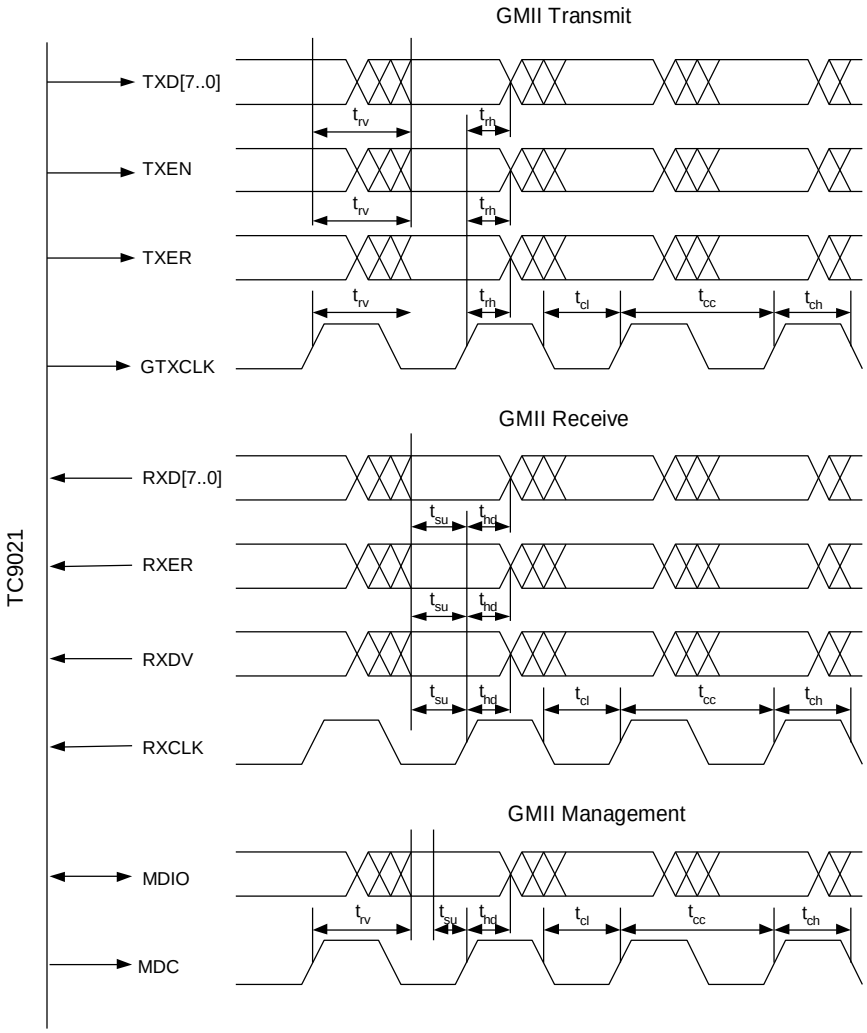
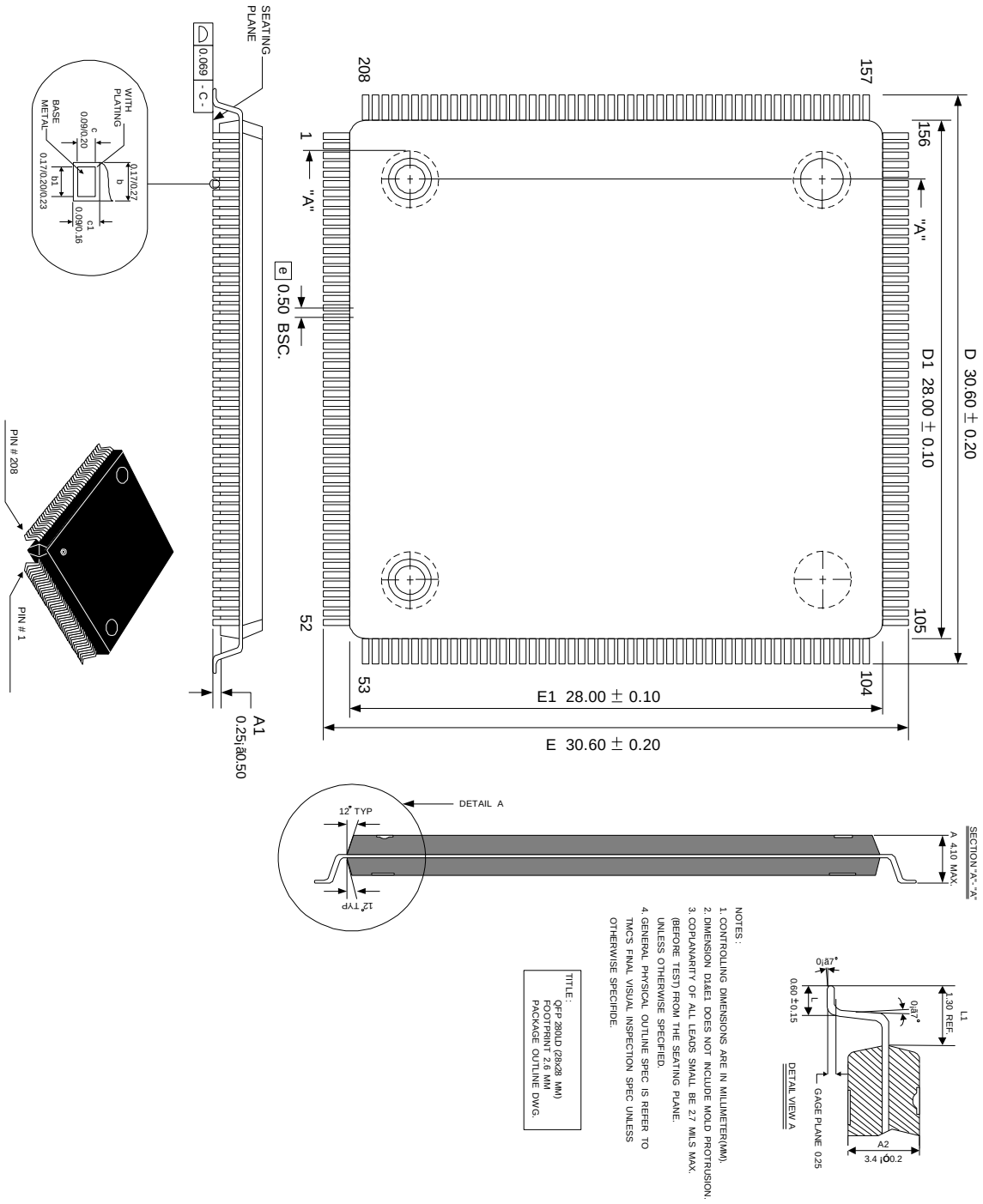


FIGURE 14: GMII Switching Characteristics



13 Physical Dimensions



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