



### General Description

The ADM 8511, USB based chipset, provides desktop, notebook and computer peripheral with greater connectivity to ethernet and home network. In the meantime, the ADM 8511 also combined a low power and small package design which is ideal for power and space constrained environment. Then, it can reduced the external component BOM cost to a minimum.

The ADM 8511 device combines a on-chip USB command & EP decoder used for USB interface through SIE ( Series Interface Engine ) , FIFO controller with 24 K SRAM, 64 byte and 2K byte buffers, 10/100 Mbps ethernet physical layer (PHY) and 1M / 10M HomePNA interface 1M8 / 10M8. The 10M HomePNA interface is MII is the same as the ethernet MAC interface. The ADM8511 is fully compliant with the IEEE 802.3u and HomePNA (Home Phoneline Network Alliance) specification revision 1.0.

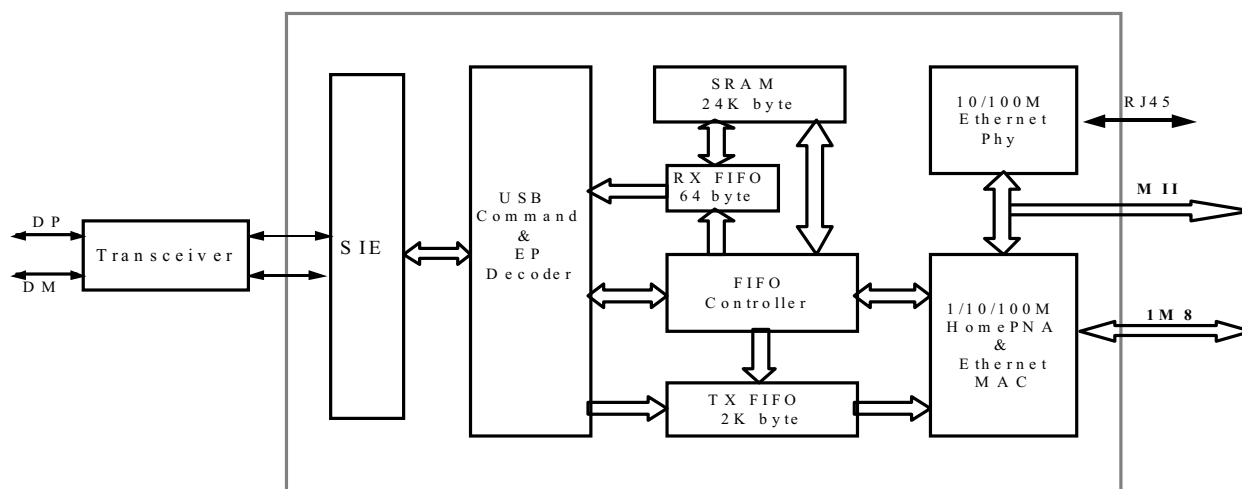
The ADM 8511 is capable of providing a easy, universal connectivity to computer peripherals with USB. The transfer rate of USB interface is 12 Mbps belonging to a high speed USB device. The ADM 8511 supports all USB commands, 4 endpoints and suspend/resume function.

The ADM 8511's LAN PHY supports 100 Base TX (100 Mbps mode) and 10 Base T (10Mbps mode) full-duplex operations. It uses the auto-negotiation function to optimize the network traffic and the built-in 24M SRAM for receiving buffer, especially for 100Mbps. Through FIFO controller, data can communicate influ rently

between buffers and external device. To obtain the better signal quality, the PHY provides wave-shaper, filter and adaptive equalizer to reach. By using diagnostic mechanism (loop-back mode), the data correctness will be increased. The Lan PHY supports external transmit/receive transformer turn ratio 1:1. The ADM8511 chipset can be programmed MAC analysis and provides MII interface for external PHY, such as 10M8 interface for 1Mbps HomePNA. In system application, EEPROM is essential that it needs to load device ID , vendor ID automatically. So for ADM 8511, serial interface is applied for EEPROM communication including read/write function. Furthermore, system statuses are reported by some LED pins including transfer speed LEDSP (100Mbps or 10Mbps), Link status (LEDL) on network and transfer type LEDFD/COL) full-duplex or half-duplex or collision on network.

ADM 8511 is ideally suited for USB adapter and intelligent networked peripheral design. By fiber media, ADM 8511 can associate with fiber tranceiver & PHY through MII interface to network in fiber network. In HomePAN application, ADM 8511 can provide 1M8 interface and 10M8 ( MII interface) associated with external 1M&10M Home PHY for 1Mbps & 10Mbps network. ADM 8511 can't apply only in LAN( Local Area Network) but also in WAN( Wide Area Network), such as xDSL, Cable Modem, and router ... e.t.c.. In IA ( Information Appliance ) application, Set-Top box is an example of ADM 8511 application. ADM 8511 also provide

### Block Diagram



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serial interface for EEPROM storing default values, e.g. vendor ID, Product ID, ...e.t.c.(EEPROM Access Program). Specially, ADM 8511 can be tested by test program (MFG) in the less time for mass production of system board level. This chip provides low power 0.35um, 3.3V/5V I/Otolerance, and 100 pin LQFP package

In software, ADM 8511 provides a fully software support, NDIS 5 driver, Linux driver, EEPROM burn-in program and MFG program. The NDIS 5 and Linux drivers are windows netware drivers. EEPROM burn-in program is convenient for customers to implement. The MFG program is a powerful tool in mass – production.



### Features

#### ● Industry Standard

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Support for IEEE 802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- USB specification 1.0 and 1.1 compliant

#### ● USB I/F

- Full-Speed USB Device
- Supports 1 USB configuration and 1 interface
- Supports all USB standard commands
- Supports two vendor specific commands
- Supports USB Suspend/Resume detection logic
- Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet

#### ● MAC/Phy

- Integrates the whole physical layer functions of 100BASE-TX and 10BASE-T by using phy address 1
- Be programmed to isolate the internal PHY, the I/F to external PHY could be either IEEE 802.3 MII (10M8 for HomePNA 2.0). Supports configurable threshold for transmitting PAUSE frame
- Supports wakeup frame, link status change and magic packet wake-up
- Provides full-duplex operation on both 100Mbps and 10Mbps Ethernet modes

- Provides Auto-negotiation(NWAY) function of full/half duplex operation for both 10/100 Mbps
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides MLT-3 transceiver with DC restoration for Base-Line Wander compensation
- Provides MAC and Transceiver loop-back modes for diagnostic
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1

#### ● EEPROM I/F

- Provides serial interface for read/write 93C46 EEPROM
- Automatically loads device ID, vendor ID from EEPROM after power-on reset

#### ● FIFO

- Supports internal 2K bytes SRAM for transmission
- Supports external 32K bytes SRAM or internal 24K bytes synchronous SRAM for receiving.
- Supports “receive 32 packets” or “receive 16 packets” queue in the receive buffer

#### ● LED Display

- Provide LED display
- LEDSP: Speed - 100Mbps(on) or 10Mbps(off)
- LEDL: Link(keeps on when link ok) or Active(will be blinking with 10Hz)
- LEDFD/COL: FD(keeps on when in Full duplex mode) or Collision(will be blinking with 20Hz when colliding)

#### ● Miscellaneous

- Support 6 GPIO pins
- Provides 100-pin LQFP package
- 3.3V power supply with 5V/3.3V I/O tolerance

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### ● **LAN Driver Support**

- Windows Networks : NDIS 5.0
- Linux

### ● **Utility**

- EEPROM burn-in program
- MFG testing program

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### Revision History

Release Date	Revision	Description
July 2000	0.1	Draft product spec for review
September 2000	1.0	Rearrange
October 2000	2.0	add appendix
December 2000	2.01	P.62 Appendix 5/item 7/item b/item ii/ TXER change to RXER
December 2000	2.02	Add max. power consumption P.1 I <sup>2</sup> C change to serial

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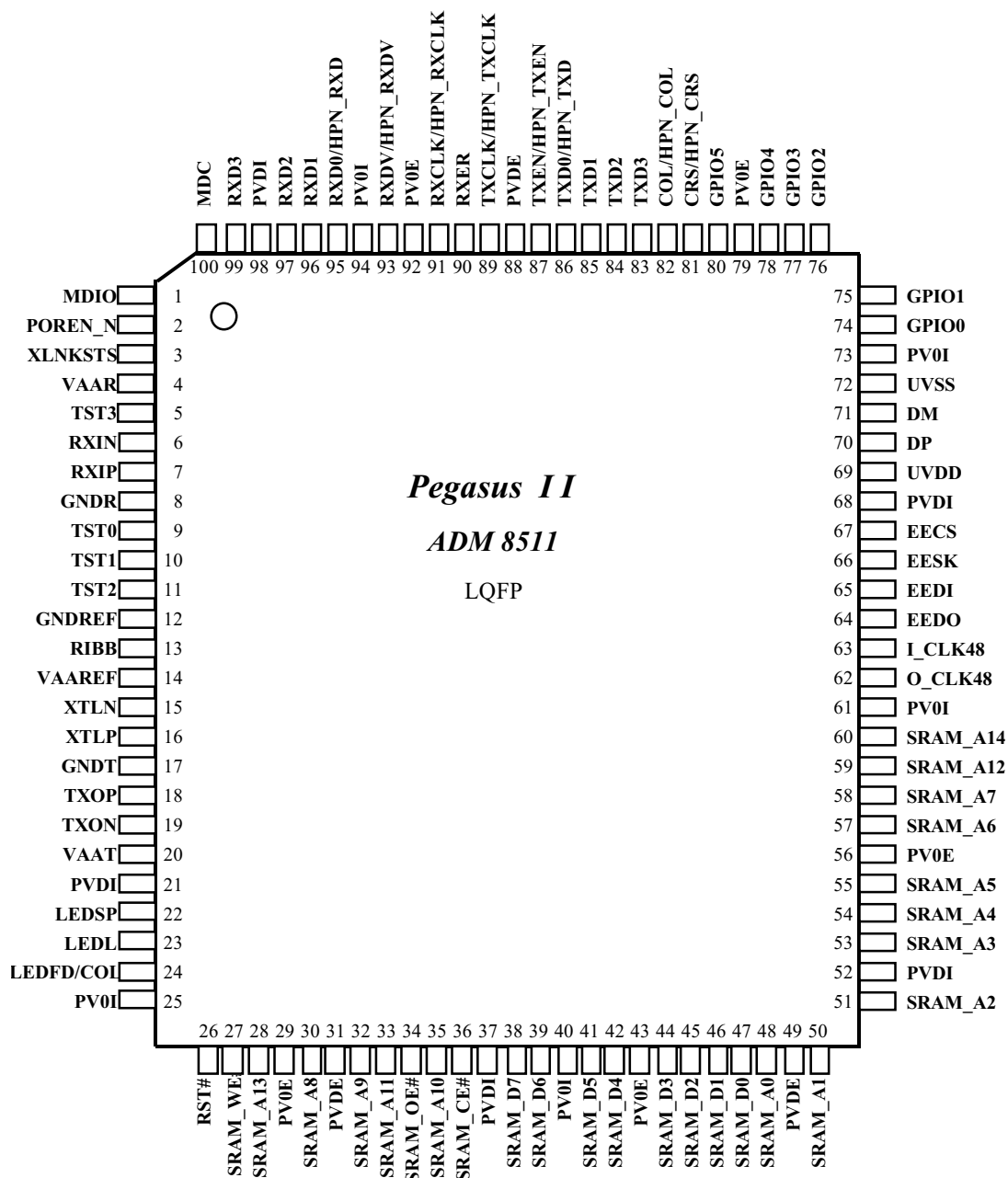
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<b>General Description</b>	1
<b>Block Diagram</b>	1
<b>Features</b>	3
<b>LAN Driver Support</b>	4
<b>Utility</b>	4
<b>Pin Assignment Diagram</b>	7
<b>Pin Descriptions</b>	8
<b>Functional Descriptions</b>	14
<b>USB Interface</b>	14
<b>MAC Interface</b>	14
<b>FIFO Controller</b>	16
<b>TX FIFO and RX FIFO</b>	17
<b>1/10/100 Ethernet/HomePNA MAC</b>	17
<b>10/100M Ethernet PHY</b>	17
<b>Register Descriptions</b>	18
<b>System register set</b>	18
<b>Transceiver register set</b>	28
<b>Electrical Specifications and Timings</b>	38
<b>Package</b>	46
<b>Appendix 1 Layout Guide</b>	48
<b>Appendix 2 EEPROM Interface &amp; Example</b>	52
<b>Appendix 3 USB Device Operation</b>	54
<b>Appendix 4 USB Command</b>	56
<b>Appendix 5 Application Notes for Ethernet Application</b>	62

#### Pin Assignment Diagram



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### ● Pin Description

Pin Name	Pin #	Type	Pin Description
<b>● Host Interface</b>			
I_CLK48	63	I	48Mhz Clock Input from crystal or oscillator.
O_CLK48	62	O	Output for crystal.
RST#	26	I	External Hardware Reset Input
DM	71	I/O	USB Data Minus pin.
DP	70	I/O	USB Data Plus pin.
<b>● MII Interface (Program ADM8511 as MAC-only mode, set 81h[4:2]=001b and 01h bit 2 = 0)</b>			
COL	82	I	<b>Collision Detected</b> This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
CRS	81	I	<b>Carrier Sense</b> This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.
MDC	100	O	<b>Management Data Clock</b> Clock signal with a maximum rate of 2.5MHz used to transfer management data for the external PMD on the MDIO pin.
MDIO	1	I/O	<b>Management Data I/O</b> Bi-directional signal used to transfer management information for the external PMD. Requires external 1.5k pull-up resistor.
RXCLK	91	I	<b>Receive Clock</b> A continuous clock that is recovered from the incoming data. During 100Mb/s operation RXCLK is 25MHz, during 10Mb/s this is 2.5MHz and during 1Mb/s operation this is 0.25MHz.



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RXD[3:0]	95-97, 99	I	<p><b>Receive Data</b></p> <p>This is a group of 4 data signals aligned on nibble boundary which are driven synchronous to the RXCLK by the external physical unit. RXD[3] is the most significant bit and RXD[0] is the least significant bit.</p>
RXDV	93	I	<p><b>Receive Data Valid</b></p> <p>This indicates that the external physical unit is presenting recovered and decoded nibbles on the RXD[3:0] and that RXCLK is synchronous to the recovered data.</p>
RXER	90	I	<p><b>Receive Error</b></p> <p>This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted. If no used, it should be grounded, <i>e.g. isolate internal phy and use external phy. However, if the external phy has RXER pin, the RXER of ADM8511 should connect to this RXER of the external phy.</i></p>
TXCLK	89	I	<p><b>Transmit Clock</b></p> <p>A continuous clock that is source by the physical layer. During 100 Mb/s operation this is 25MHz <math>\pm</math>100 ppm. During 10 Mb/s operation this clock is 2.5MHz <math>\pm</math>100 ppm. During 1 Mb/s operation this clock is 0.25MHz <math>\pm</math>100 ppm.</p>
TXD[3:0]	83,84, 85,86	O	<p><b>Transmit Data</b></p> <p>This is a group of 4 data signals which driven synchronously to the TXCLK for transmission to the external physical unit. TXD[3] is the most significant bit and TXD[0] is the least significant bit.</p>
TXEN	87	O	<p><b>Transmit Enable</b></p> <p>This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TX[3:0] contains valid data to be transmitted. <i>Require external pull-down resistor 4.7K if external phy is used</i></p>



XLNKSTS	3	I	<b>Link Status Indication</b> Link status indication External PHY reports link status information to system and level change trigger. <b>Pull-down to low if external phy is used.</b>
<b>● 1M8 Interface (Program ADM8511 as MAC-only mode, set 81h[4:2]=001b and 01h bit 2 = 1)</b>			
HPN_COL	82	I	<b>Collision</b> Indicates a collision was detected by the 1M8 PHY on the 1M8 wiring network.
HPN_CRS	81	I	<b>Carrier Sense</b> Indicates the 1M8 PHY is receiving a valid 1M8 signal from the wiring network.
HPN_RXCLK	91	I	<b>Receive Clock</b> Clock for RX_D.
HPN_RXD	95	I	<b>Receive Data</b> Data to the MAC is synchronously clocked by HPN_RXCLK.
HPN_RXDV	93	I	<b>Receive Data Valid</b> This indicates that the external physical unit is presenting recovered and decoded nibbles on the HPN_RXD and that HPN_RXCLK is synchronous to the recovered data.
HPN_TXCLK	89	I	<b>Transmit Clock</b> Clock for HPN_TXD.
HPN_TXD	86	O	<b>Transmit Data</b> Data to the PHY is synchronously clocked by HPN_TXCLK.
HPN_TXEN	87	O	<b>Transmit Enable</b> Transmit enable request from the MAC to begin sending data to the PHY.
<b>● Physical Interface</b>			
XTLP, XTLN	16, 15	I	Crystal inputs. To be connected to a 25MHz crystal.

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RXIN, RXIP	6, 7	I	The differential receive inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic.
TXOP, TXON	18, 19	O	The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic.
RIBB	13	I	Reference Bias Resistor. To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end.
TST0, TST1, TST2, TST3	9, 10, 11, 5	I	Test pin
<b>● LED display</b>			
LEDSP	22	O	LED display for 100M b/s or 10M b/s speed. Active low indicates 100Base-TX, active high indicates 10 BaseT.
LEDL	23	O	LED display for link and activity status. Active low when link is established.
LEDFD/COL	24	O	LED display for Full Duplex or Collision status. Active low indicates full duplex, high indicates collision in half duplex.
<b>● SRAM Interface</b>			
SRAM_A[14:0]	48, 50, 51, 53, 54, 55, 57, 58, 30, 32, 35, 33, 59, 28, 60	O	External SRAM Address Bus
SRAM_D[7:0]	47, 46, 45, 44, 42, 41, 39, 38	I/O	External SRAM Data Bus Internal pull down

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SRAM_CE#	36	O	External SRAM Chip Enable
SRAM_OE#	34	O	External SRAM Output Enable.
SRAM_WE#	27	O	External SRAM Write Enable.
<b>● EEPROM Interface</b>			
EECS	67	O	<b>EEPROM Chip Select</b> This enables the EEPROM during loading of the Ethernet configuration data.
EEDI	65	O	<b>EEPROM Data In</b> The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM.
EEDO	64	I	<b>EEPROM Data Out</b> The MAC will read the contents of the EEPROM serially through this pin.
EESK	66	O	<b>EEPROM Clock</b> After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM.
<b>● Miscellaneous</b>			
GPIO[5:0]	80, 78, 77, 76, 75, 74	I/O	These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM. Default is internal pull-low
POREN_N	2	I	Internal Power On Reset Logic Enable. Default is enable and internal pull - low. When external hardware reset is used, this pin should be connected to Vcc via 4.7k resistor.
<b>● Power Pins</b>			
PVDI	21, 37, 52, 68, 98	P	3.3v power supply for core.
PVDE	31, 49, 88	P	3.3v power supply for pads.
PV0I	25, 40, 61, 73, 94	P	Ground for PVDI
PV0E	29, 43,	P	Ground for PVDE

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UVDD	69	P	3.3v power supply for USB transceiver
UVSS	72	P	Ground for UVDD
VAAR, VAAREF, VAAT	4, 14, 20	P	Analog Power Pins, 3.3v
GNDR, GNDREF, GNDT	8, 12, 17	P	Analog Ground Pins

### Function Descriptions

- **USB Interface**

USB is likely solution any time you want to use a computer to communication with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced, standard peripheral. The benefits to USB are ease of use, fast and reliable data transfers, flexibility, low cost and power conservation.

#### **SIE**

SIE (Serial Interface Engine) is to control USB communications and check USB protocol, then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine.

#### **USB Command & EP Decoder**

The detail description is in Appendix 4.

- **MAC Interface**

#### **MII**

The Media Independent Interface (MII) is an 18 wire MAC/Phy interface described in 802.3u. The purpose of the interface is to allow MAC layer devices to attach to a variety of Physical Layer devices through a common interface. MII operates at either 100Mbps or 10Mbps, dependant on the speed of the Physical Layer. With clocks running at either 25 MHz or 2.5 MHz, 4 bit data is clocked between the MAC and Phy, synchronous with Enable and Error signals.

On receipt of valid data from the wire interface, RX\_DV will go active signaling to the MAC that the valid data will be presented on the RXD[3:0] pins at the speed of the RX\_CLK.

On transmission of data from the MAC, TX\_EN is presented to the phy indicating the presence of valid data on TXD[3:0]. TXD[3:0] are sampled by the phy synchronous to TX\_CLK during the time that TX\_EN is valid.

#### **Adaptive Equalizer**

The amplitude and phase distortion from cable cause inter-symbol interference (ISI) which makes clock and data recovery difficult. The adaptive equalizer is designed to closely match the inverse transfer function of the twisted-pairs cable. The equalizer has the ability to change its equalizer frequency response according to the cable length. The

equalizer will tune itself automatically for any cable, compensating for the amplitude and phase distortion introduced by the cable.

#### **LEDs**

Individual LED output are available to indicate Speed, Duplex, Collision, Transmit, and Link. These multi-function pins are inputs during reset and LED output pins thereafter. The level of these pins during reset determines their active output states. If a multi-function pin is pulled up during reset to select a particular function, then that LED output would become active low, and the LED circuit must be designed accordingly, and vice versa.

#### **Jabber and SQE**

After the MAC transmitter exceeds the jabber timer, the transmit and loopback functions will be disabled and COL signal get asserted. After TX\_EN goes low for more than 500ms, the TP transmitter will reactivate and COL gets de-asserted. Setting Jabber Disable will disable the jabber function.

When the SQE test is enabled, a COL pulse is asserted after each transmitted packet. SQE is enabled in 10Base-T by default.

#### **Auto Polarity**

Certain cable plants have crossed wiring on the twisted pairs; the reversal of TXIN and TXIP. Under normal circumstances this would cause the receive circuitry to reject all data. When the Auto Polarity Disable bit is cleared, the Phy has the ability to detect the fact that either 8 NLPs (normal link pulse) or a burst of FLPs are inverted and automatically reverse the receiver's polarity. The polarity state is stored in the Reverse Polarity bit.

#### **Auto-Negotiation**

It provides a linked device with the capability to detect the abilities (modes of operation) supported by the device at the other end of the link, determine common abilities, and configure for joint operation. Auto-Negotiation is performed out-of-band using a pulse code sequence that is compatible with the 10BASE-T link integrity test sequence.

### Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC components of the incoming signal, thus the DC offset of the differential receive inputs can drift. The shifting of the signal level, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion. This creates jitter and possible increase in the bit error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of the DC component. Unlike the traditional implementation, the circuit does not need the feedback information from the slicer or the clock recovery circuit. The design simplifies the circuit design. In 10BASE-T, the baseline wander correction circuit is not required.

### ● FIFO Controller

FIFO Controller in receive path is in charge of:

- (1) Store received Ethernet packets to SRAM (internal 24Kbyte or external 32Kbyte) and total 32 (or 16) packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than 32K (or 24K for internal SRAM) bytes, the subsequent coming Ethernet packet will be discarded.
- (2) FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller inform this, any USB access to bulk IN endpoint will return NAK. This is to maintain the data transfer on USB bus via bulk IN transfer is continuous, thus a 64-byte internal RX FIFO is needed.
- (3) If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

FIFO Controller in transmit path is in charge of:

- (1) Store each individual USB packet to internal TX FIFO. When EP decoder informs end of packet, a complete Ethernet packet is stored in TX FIFO. FIFO Controller then informs MAC to transmit this packet.
- (2) Total 4 Ethernet packets can be stored in TX FIFO. If all 4 Ethernet packet are stored in TX FIFO or total packet size is more than 2K bytes, FIFO Controller will inform EP Decoder that TX FIFO is full and EP Decoder will return NAK if accessing to bulk OUT endpoint is invoked. Thus additional USB packet won't be written into TX FIFO until TX FIFO has free space.



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- **TX FIFO and RX FIFO**

RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2K-byte FIFO.

- **1/10/100 Ethernet/HomePNA MAC**

The MAC controller takes in charge of

- (1) Generate CRC then transmit Ethernet packet.
- (2) Check CRC for received packet CRC, filter the received packets.
- (3) Polling PHY status.
- (4) Magic packet detection.
- (5) Automatically transmit PAUSE frame when received status meets the flow control criteria.
- (6) Late collision transmit packets will be discarded.

- **10/100M Ethernet PHY**

The internal Ethernet PHY is compliant to IEEE 802.3u 100BASE-TX and IEEE802.3 10BASE-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed. The internal PHY can be isolated by programming register offset 7Bh, bit 1.



- **Register Descriptions**

- **System Register Table**

Offset	Register
00-02h	Ethernet control registers
03-07h	Reserved
08-0Fh	Multicast address table registers
10-15h	Ethernet ID registers
16-17h	Reserved
18-19h	Pause timer registers
1Ah	Receive packet number based flow control register
1Bh	Occupied receive FIFO based flow control register
1Ch	EP1 control register
1Dh	RX FIFO control register
1Eh	BIST control register
1Fh	Reserved
20h	EEPROM offset register
21-22h	EEPROM data registers
23h	EEPROM access control register
24h	Reserved
25h	PHY address register
26-27h	PHY data registers
28h	PHY access control register
29h	Reserved
2Ah	USB status register
2B-2Ch	Ethernet transmit status registers
2Dh	Ethernet receive status register
2E-2Fh	Ethernet receive lost packet count register
30-3Fh	Wakeup frame 0 mask registers
40h	Wakeup frame0 offset register
41-42h	Wakeup frame0 CRC registers
43-47h	Reserved
48-57h	Wakeup frame 1 mask registers
58h	Wakeup frame 1 offset register
59-5Ah	Wakeup frame 1 CRC registers
5B-5Fh	Reserved
60-6Fh	Wakeup frame 2 mask registers
70h	Wakeup frame 2 offset register
71-72h	Wakeup frame 2 CRC registers
73-77h	Reserved
78h	Wakeup control register
79h	Reserved
7Ah	Wakeup status register
7Bh	Internal PHY control register
7Ch	GPIO[5:4] control register
7Dh	Reserved
7Eh	GPIO[1:0] control register
7Fh	GPIO[3:2] control register
80h	TEST register
81h	Test mode register
82-FFh	Reserved



● **Offset 00h: Ethernet control\_0**

Bit	Field	HW Access	SW access	Default value	Description
7	tx_en	R	R/W	0	Enable Ethernet transmission.
6	rx_en	R	R/W	0	Enable Ethernet receive.
5	rx_flowctl_en	R	R/W	0	Enable receive pause frame.
4	wakeon_en	R	R/W	0	Enable wake-on-LAN mode.
3	rxstatus_append	R	R/W	1	Enable status append at the end of received packet.
2	stop_back_off	R	R/W	0	1: back-off counter stop when carrier is active and resume when carrier drop. 0: back-off counter isn't affected by carrier.
1	rx_multicast_all	R	R/W	0	Receive all multicast packet
0	rx_crc_sent	R	R/W	1	Include CRC in receive packet.

● **Offset 01h: Ethernet control\_1**

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6	delay_home	R	R/W	0	1: 1bit data is dropped after HPN_CRS asserts. 0: all data is received after HPN_CRS asserts.
5	full_duplex	R	R/W	0	1: full-duplex mode. 0: half-duplex mode.
4	10mode	R	R/W	0	0: 10Base-T mode. 1: 100Base-T mode.
3	reset_mac	R	R/W	0	Reset MAC, After write 1, HW will clear this bit after MAC reset.
2	homelan_mode	R	R/W	0	1: 1M8 I/F to external PHY 0: MII I/F to external PHY
0-1	reserved				

● **Offset 02h: Ethernet control\_2**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	load EEPROM start	R	R/W	0	When this bit is written with 1, HW will start to load EEPROM.
4	EEPROM write enable/disable	R	R/W	0	1: EEPROM write command 0: EEPROM write enable/disable command
3	loop_back	R	R/W	0	Enable MAC loop back mode
2	promiscuous	R	R/W	0	1: receive any packet. 0: receive packets which pass the address filter.
1	rx_bad_pkt	R	R/W	0	1: receive bad packets which pass the address filter. 0: filter all bad packet
0	Ep3_rd_clr/	R	R/W	0	1: Once EP3 is accessed, those registers(2B-2F, 7A) will be cleared. 0: Access EP3, no effect to those registers.



- **Offset 03-07h: reserved**

- **Multicast address**

offset	Bit	Field	HW access	SW access	Default value	Description
08h	7-0	Multicast0	R	R/W	0	Multicast address byte 0 (hash table[7:0]).
09h	7-0	Multicast1	R	R/W	0	Multicast address byte 1 (hash table[15:8]).
0Ah	7-0	Multicast2	R	R/W	0	Multicast address byte 2 (hash table[23:16]).
0Bh	7-0	Multicast3	R	R/W	0	Multicast address byte 3 (hash table[31:24]).
0Ch	7-0	Multicast4	R	R/W	0	Multicast address byte 4 (hash table[39:32]).
0Dh	7-0	Multicast5	R	R/W	0	Multicast address byte 5 (hash table[47:40]).
0Eh	7-0	Multicast6	R	R/W	0	Multicast address byte 6 (hash table[55:48]).
0Fh	7-0	Multicast7	R	R/W	0	Multicast address byte 7 (hash table[63:56]).

- **Ethernet ID**

Offset	Bit	Field	HW access	SW access	Default value	Description
10h	7-0	Etherid0	R/W	R/W	0	The 1st byte of ethernet ID is automatically loaded from EEPROM after HW reset.
11h	7-0	Etherid1	R/W	R/W	0	The 2nd byte of ethernet ID.
12h	7-0	Etherid2	R/W	R/W	0	The 3rd byte of ethernet ID.
13h	7-0	Etherid3	R/W	R/W	0	The 4th byte of ethernet ID.
14h	7-0	Etherid4	R/W	R/W	0	The 5th byte of ethernet ID.
15h	7-0	Etherid5	R/W	R/W	0	The 6th byte of ethernet ID.

- **Offset 16-17h: reserved**

- **Offset 18h: pause\_timer low**

Bit	Field	HW access	SW access	Default value	Description
7-0	pause_timer	R	R/W	0F	The [11:4] of pause time in the PAUSE frame.

- **Offset 19h: reserved**

- **Offset 1Ah: receive packet number based flow control**

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6-1	pkt_no	R	R/W	6'h0F	This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW.
0	flowctl_pkt	R	R/W	0	Enable pause frame transmission bases on receive packet number.



● **Offset 1Bh: occupied receive FIFO based flow control**

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6-1	rxsize	R	R/W	6'h0F	This field specifies the K byte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field =2, as receive FIFO is occupied more than or equal to 2K byte, the PAUSE frame is transmitted.
0	flowctl_rxsize	R	R/W	0	Enable pause frame transmission bases on occupied receive FIFO size.

● **Offset 1Ch: EP1 Control**

Bit	Field	HW access	SW access	Default value	Description
7	ep1_send0_en	R	R/W	0	1: enable EP1 send 1-byte 00 when more than frame_interval's NAK is received 0: disable EP1 send 1-byte 00 function
6-5	test_itvl_a	R	R/W	2'd0	This value are used for internal test mode.
4-0	test_itvl_b	R	R/W	5'd0	This value are used for internal test mode.

● **Offset 1Dh: RX FIFO Control**

Bit	Field	HW Access	SW access	Default value	Description
7-2	reserved				
1	ext_sram_en	R	R/W	0	1: supports external 32K-byte SRAM 0: supports internal 24K-byte SRAM
0	rx32pkt	R	R/W	0	1: support maximum 32 packets in receive FIFO 0: support maximum 16 packets in receive FIFO

● **Offset 1Eh: BIST control**

Bit	Field	HW Access	SW access	Default value	Description
7-3	reserved				
2	bist_result	R/W	R	0	This bit indicated the bist result and is valid when "bist_test_done" is '1'. This bit also reflects the value of "pass_or_fail" signal in BIST module. 1: pass 0: fail
1	bist_test_done	R/W	R	0	This bit indicates the completion of bist. The bist completes if this bit is '1'. This bit also reflects the value of "test_done" signal in BIST module.
0	bist_en_n	R	R/W	1	This bit enable the BIST function and also drives the "reset" signal in BIST module. 1: disable BIST function 0: enable BIST function

# ADMtek Incorporated

## ADM 8511

Pegasus II

USB / Fast Ethernet / HomePNA Controller



### ● Offset 20h: EEPROM offset

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5-0	rom_offset	R	R/W	0	SW sets this register when access to EEPROM.

### ● Offset 21h: EEPROM data low

Bit	Field	HW access	SW access	Default value	Description
7-0	romdata_lo	R/W	R/W	0	SW sets this register when writes to EEPROM. HW sets this register when read data from EEPROM.

### ● Offset 22h: EEPROM data high

Bit	Field	HW access	SW access	Default value	Description
7-0	romdata_hi	R/W	R/W	0	SW sets this register when writes to EEPROM. HW sets this register when reads data from EEPROM.

### ● Offset 23h: EEPROM access control

Bit	Field	HW access	SW access	Default value	Description
7-3	reserved				
2	done	R/W	R/W	0	Set by HW to indicate successful completion of EEPROM access. Clear by SW when initiate a new access to EEPROM
1	rd_eeeprom	R	R/W	0	Set by SW to initiate a read access to EEPROM. SW sets this bit after it well setting the rom_offset.
0	wr_eeeprom	R	R/W	0	Set by SW to initiate a write access to EEPROM. SW set this bit after it well setting the rom_offset, romdata_lo and romdata_hi.

### ● Offset 24h: reserved

### ● Offset 25h: PHY address

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-0	phy_addr	R	R/W	0	MII PHY address.

### ● Offset 26h: PHY data low

Bit	Field	HW access	SW access	Default value	Description
7-0	phydata_low	R/W	R/W	0	SW set this register when write to phy registers. HW set this register when read data from PHY register.



● **Offset 27h: PHY data high**

Bit	Field	HW access	SW access	Default value	Description
7-0	phydata_high	R/W	R/W	0	SW set this register when write to phy registers. HW set this register when read data from PHY register.

● **Offset 28h: PHY access control**

Bit	Field	HW access	SW access	Default value	Description
7	done	R/W	R/W	0	Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.
6	rd_phy	R	R/W	0	Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.
5	wr_phy	R	R/W	0	Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data.
4-0	phyreg_addr	R	R/W	0	PHY register address.

● **Offset 29h: reserved**

● **Offset 2Ah: usb bus status**

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	usb_resume	R/W	R/W	0	Set by HW to indicate usb bus in resume state. Clear by SW read this register.
0	usb_suspend	R/W	R/W	0	Set by HW to indicate usb bus in suspend state. Clear by SW read this register.

● **Offset 2Bh: transmit status\_1**

Bit	Field	HW access	SW access	Default value	Description
7	txunderrun	R/W	R	0	Set by HW to indicate tx underrun error. Clear by SW read this register or after EP3 is accessed.
6	excessive_col	R/W	R	0	Set by HW to indicate excessive collision. Clear by SW read this register or after EP3 is accessed.
5	late_col	R/W	R	0	Set by HW to indicate late collision error. Clear by SW read this register or after EP3 is accessed.
4	no_carrier	R/W	R	0	Set by HW to indicate no carrier. Clear by SW read this register or after EP3 is accessed.
3	loss_carrier	R/W	R	0	Set by HW to indicate carrier loss. Clear by SW read this register or after EP3 is accessed.
2	jabber_timeout	R/W	R	0	Set by HW to indicate jabber time out. Clear by SW read this register or after EP3 is accessed.
1-0	reserved				



● **Offset 2Ch: transmit status\_2**

Bit	Field	HW access	SW access	Default value	Description
7	txfifo_full	R/W	R	0	Set by HW to indicate tx fifo full. Clear by SW read this register or after EP3 is accessed.
6	txfifo_empty	R/W	R	0	Set by HW to indicate tx fifo empty. Clear by SW read this register or after EP3 is accessed.
5-4	reserved				
3-0	txpkt_cnt	R/W	R	0	Set by HW to indicate Ethernet transmit packet count every interrupt EP polling. If more than 15 packets have been transmitted, this value will keep as 15. Clear by SW read or after EP3 is accessed.

● **Offset 2Dh: receive status**

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	rx_pause	R/W	R/W	0	Set by HW to indicate a PAUSE frame is received. Clear by SW read this register or after EP3 is accessed.
0	rx_overflow	R/W	R	0	Set by HW to indicate external SRAM overflow. Clear by SW read this register or after EP3 is accessed.

● **Offset 2Eh: receive lost packet count high**

Bit	Field	HW access	SW access	Default value	Description
7	Lostpkt	R/W	R/W	0	
6-0	rx_lostpkt	R/W	R/W	0	The [14:8] of lost packet counts due to receive FIFO overflow. Clear by SW read this register or after EP3 is accessed.

● **Offset 2Eh: receive lost packet count low**

Bit	Field	HW access	SW access	Default value	Description
7-0	rx_lostpkt	R/W	R/W	0	The [7:0] of lost packet counts due to receive FIFO overflow. Clear by SW read this register or after EP3 is accessed.

● **Wake-up frames**

Offset	Bit	Field	HW access	SW access	Default value	Description
30-3Fh		f0_mask				The 128 mask bits for fram0.
40h	7-0	f0_offset	R	R/W	0	Offset for wakeup frame0.
41h	7-0	f0_crc_low	R	R/W	0	The low byte of CRC16 match for frame 0.



# ADMtek Incorporated

## ADM 8511

**Pegasus II**

**USB / Fast Ethernet / HomePNA Controller**



42h	7-0	f0 crc hi	R	R/W	0	The high byte of CRC16 match for frame 0.
43-47h		reserved				
48-57h		f1 mask				The 128 mask bits for fram1.
58h	7-0	f1 offset	R	R/W	0	Offset for wakeup frame1.
59h	7-0	f1 crc low	R	R/W	0	The low byte of CRC16 match for frame 1.
5Ah	7-0	f1 crc hi	R	R/W	0	The high byte of CRC16 match for frame 1.
5B-5Fh		reserved				
60-6Fh		f2 mask				The 128 mask bits for fram2.
70h	7-0	f2 offset	R	R/W	0	Offset for wakeup frame2.
71h	7-0	f2 crc low	R	R/W	0	The low byte of CRC16 match for frame 2.
72h	7-0	f2 crc hi	R	R/W	0	The high byte of CRC16 match for frame 2.
73-77h		reserved				

● **Offset 78h: wake-up control**

Bit	Field	HW access	SW access	Default value	Description
7	mgcpkt_en	R	R/W	0	Set by SW to enable magic packet wakeup function.
6	link_en	R	R/W	0	Set by SW to enable link status wakeup function.
5	wakeupframe0_en	R	R/W	0	Set by SW to enable wakeup frame0 wakeup function.
4	wakeupframe1_en	R	R/W	0	Set by SW to enable wakeup frame1 wakeup function.
3	wakeupframe2_en	R	R/W	0	Set by SW to enable wakeup frame2 wakeup function.
2	crc16type	R	R/W	1	0: CRC-16 initial contents = 0000h 1: CRC-16 initial contents = ffffh
1-0	reserved				

● **Offset 79h: reserved**

● **Offset 7Ah: wake-up status**

Bit	Field	HW access	SW access	Default value	Description
7	rx_mgcpkt	R/W	R	0	Set by HW when receive a magic packet. Clear by SW read this register.
6	link_wake	R/W	R	0	Set by HW when link status change. Clear by SW read this register.
5	rx_wakeupframe	R/W	R	0	Set by HW when receive a wakeup frame. Clear by SW read this register.
4-1	reserved				
0	link_sts	R/W	R	0	Indicate the current link status, 1 for link on, 0 for link off.

● **Offset 7B: internal PHY control**

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	power_down_phy	R	R/W	0	0: power down internal 10/100 PHY 1: enable internal 10/100 PHY
0	phyrst	R	R/W	0	1: Reset internal PHY The internal PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0.

# ADMtek Incorporated

## ADM 8511

Pegasus II

USB / Fast Ethernet / HomePNA Controller



● **Offset 7Ch: GPIO[5:4]**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO5_oe	R	R/W	0	GPIO5 output enable. 1: GPIO5 is used for output 0: GPIO5 is used for input
4	GPIO5_o	R	R/W	0	GPIO5 output value. When GPIO5 is used for output, this value is driven to GPIO5 pin. Set by SW.
3	GPIO5_i	R/W	R		GPIO5 input value. When GPIO5 is used for input, this field reflects the status of GPIO5. Default is pulled-down.
2	GPIO4_oe	R	R/W	0	GPIO4 output enable. 1: GPIO4 is used for output 0: GPIO4 is used for input
1	GPIO4_o	R	R/W	0	GPIO4 output value. When GPIO4 is used for output, this value id driven to GPIO4 pin. Set by SW.
0	GPIO4_i	R/W	R		GPIO4 input value. When GPIO4 is used for input, this field reflects the status of GPIO4. Default is pulled-down.

● **Offset 7Eh: GPIO[1:0]**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO1_oe	R	R/W	0	GPIO1 output enable. 1: GPIO1 is used for output 0: GPIO1 is used for input
4	GPIO1_o	R	R/W	0	GPIO1 output value. When GPIO1 is used for output, this value id driven to GPIO1 pin. Set by SW.
3	GPIO1_i	R/W	R		GPIO1 input value. When GPIO1 is used for input, this field reflects the status of GPIO1. Set by HW.
2	GPIO0_oe	R	R/W	0	GPIO0 output enable. 1: GPIO0 is used for output 0: GPIO0 is used for input
1	GPIO0_o	R	R/W	0	GPIO0 output value. When GPIO0 is used for output, this value id driven to GPIO0 pin. Set by SW.
0	GPIO0_i	R/W	R		GPIO0 input value. When GPIO0 is used for input, this field reflects the status of GPIO0. Set by HW.



● **Offset 7Fh: GPIO[3:2]**

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO3_oe	R	R/W	0	GPIO3 output enable. 1: GPIO3 is used for output 0: GPIO3 is used for input
4	GPIO3_o	R	R/W	0	GPIO3 output value. When GPIO3 is used for output, this value is driven to GPIO3 pin. Set by SW.
3	GPIO3_i	R/W	R		GPIO3 input value. When GPIO3 is used for input, this field reflects the status of GPIO3. Set by HW.
2	GPIO2_oe	R	R/W	0	GPIO2 output enable. 1: GPIO2 is used for output 0: GPIO2 is used for input
1	GPIO2_o	R	R/W	0	GPIO2 output value. When GPIO2 is used for output, this value is driven to GPIO2 pin. Set by SW.
0	GPIO2_i	R/W	R		GPIO2 input value. When GPIO2 is used for input, this field reflects the status of GPIO2. Set by HW.

● **Offset 80h: TEST Register**

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-1	group_sel	R	R/W	0	Internal probing signal group selection.
0	usb_test	R	R/W	0	0: 6 test pins are used for USB transceiver. 1: 6 test pins are used for internal signal probing.

● **Offset 81: Test Mode**

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-2	MII test_mode	R	R/W	0	This value could be update from EEPROM offset 0A[4:2]. 3'b000: tri-state MII pins 3'b001: enable MAC's MII signals to external pins 3'b010: enable PHY's MII signals to external pins 3'b011: monitor mode MII
1	USB transceiver test_mode	R	R/W	1	This value could be update from EEPROM offset 0A[1]. 1'b0: external USB transceiver, GPIO[5:0] are used as external USB transceiver interface 1'b1: Internal USB transceiver, GPIO[5:0] are used as GPIO pins.
0	reserved				



#### ● Transceiver Register Set

#### Transceiver registers list

Register	Description	Default
0	Control Register	1000
1	Status Register	7849
2	PHY Identifier 1 Register	0022
3	PHY Identifier 2 Register	5513
4	Auto-Negotiation Advertisement Register	01E1
5	Auto-Negotiation Link Partner Ability Register	0001
6	Auto-Negotiation Expansion Register	0004
7	Next Page Advertisement Register	2001
8-15	Reserved	XXXX
16	ADMTEK specific Register	0540
17	Interrupt Control/Status Register	0000
18	Diagnostic Register	0000
19	Power Management & Loopback Register	0020
20	Loopback and Power management Register	XXFX
21	Mode Control Register	0304
22	Reserved	XXXX
23	PLL Lock Register	0000
24	Receive Error Counter Register	0000
25-31	Reserved	XXXX



### Transceiver registers Descriptions

Legend:

Type	Description	Type	Description
RW	Readable and writable	RO	Read Only
SC	Self Clearing	RC	Cleared on the read operation
LL	Latch Low until clear	LH	Latch high until clear

### Register 0: Control Register

Reg.bit	Name	Description	Mode	Default
0.15	Reset	1 = PHY reset. This bit is self-clearing.	RW/SC	0
0.14	Loopback	1 = Enable loopback mode. This will loopback TXD to RXD, thus it will ignore all the activity on the cable media. 0 = Normal operation.	RW	0
0.13	Speed Select	1 = 100Mbps, 0 = 10Mbps. This bit will be ignored if Auto Negotiation is enabled (0.12=1).	RW	1
0.12	Auto-Neg. Enable	1 = Enable auto-negotiate process (overrides 0.13 and 0.8) 0 = Disable auto-negotiate process.	RW	1
0.11	Power Down	1 = Power down. ADM 8511 will shut off all blocks except for MDIO/MDC interface. 0 = Normal operation.	RW	0
0.10	Isolate	1 = Electrically isolate the PHY from MII. However, PHY is still able to response to MDC/MDIO. 0 = Normal operation.	RW	0
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process. 0 = Normal operation.	RW/SC	0
0.8	Duplex Mode	1 = Full duplex. 0 = Half duplex. If Auto-Neg. enabled: This bit is writable but will be ignored.	RW	0
0.7	Collision Test	1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal. 0 = disable COL test.	RW	0
0.[6:0]	Reserved		RW	0000000

### Register 1: Status Register

Reg.bit	Name	Description	Mode	Default
1.15	100Base-T4	Permanently tied to zero indicates no 100BaseT4 capability.	RO	0
1.14	100Base-TX Full Duplex	1 = 100BaseTX with full duplex. 0 = No 100BaseTX full duplex ability.	RO	1
1.13	100Base-TX Half Duplex	1 = 100BaseTX with half duplex. 0 = No TX half-duplex ability.	RO	1
1.12	10Base-T Full Duplex	1 = 10BaseT with full duplex. 0 = No 10BaseT full duplex ability.	RO	1
1.11	10Base-T Half Duplex	1 = 10BaseT with half duplex. 0 = No 10BaseT half duplex ability.	RO	1
1.[10:6]	Reserved		RO	00000
1.5	Auto-Negotiate Complete	1 = Auto-negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set. 0 = Auto-negotiate process not completed.	RO	0
1.4	Remote Fault	1 = Remote fault condition detected. 0 = No remote fault. This bit will remain set until it is cleared by reading register 1 via management interface.	RO/LH	0
1.3	Auto-Negotiate Ability	1 = Able to perform Auto-Negotiation function 0 = Unable to perform Auto-Negotiation function.	RO	1
1.2	Link Status	1 = Link is established. This is Latched bit. Therefore, if ADM8511 link failed, this bit will be cleared and remain "0" until register is read again via management interface. 0 = link is down.	RO/LL	0
1.1	Jabber Detect	1 = Jabber condition detect. 0 = No Jabber condition detected.	RO/LH	0
1.0	Extended Capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

### Register 2: PHY Identifier 1 Register

Reg.bit	Name	Description	Mode	Default
2.[15:0]	OUI	Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0382(H)



### Register 3: PHY Identifier 2 Register

Reg.bit	Name	Description	Mode	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	010010
3.[9:4]	Model Number	Six bit manufacturer's model number.	RO	000001
3.[3:0]	Revision Number	Four bit manufacturer's revision number.	RO	0000

### Register 4: Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.15	Next Page	1 = Next Page enabled. 0 = Next Page disabled.	RW	0
4.14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4.13	Remote Fault	1 = Advertises that this device has detected a Remote Fault. 0 = No remote fault detected.	RW	0
4.[12:10]	Reserved	For future technology.	RW	000
4.9	100Base-T4	this bit ties to zero.	RO	0
4.8	100Base-TX Full Duplex	1 = 100BaseTX full duplex supported by Local device. 0 = 100BaseTX full duplex not supported by Local device.  Default is set by Reg. 1.14.	RW	1
4.7	100Base-TX	1 = 100BaseTX supported by Local device. 0 = 100BaseTX not supported by Local device. Default is set by Reg. 1.13.	RW	1
4.6	10Base-T Full Duplex	1 = 10Mbps full duplex supported by Local device. 0 = 10Mbps full duplex not supported by Local device. Default is set by Reg. 1.12.	RW	1
4.5	10Base-T	1 = 10Mbps supported by Local device. 0 = 10Mbps not supported by Local device. Default is set by Reg. 1.11.	RW	1
4.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RW	00001

### Register 5: Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.15	Next Page	1 = Link partner desires Next Page transfer. 0 = Link partner does not desire Next Page transfer.	RO	0
5.14	Acknowledge	1 = Link Partner acknowledges reception of FLP words. 0 = No acknowledged by Link Partner.	RO	0

# ADMtek Incorporated

## ADM 8511

**Pegasus II**

**USB / Fast Ethernet / HomePNA Controller**



5.13	Remote Fault	1 = Remote Fault indicated by Link Partner. 0 = No remote fault detected by Link Partner.	RO	0
5.[12:10]	Reserved	For future technology.	RO	000
5.9	100Base-T4	1 = 100BaseT4 supported by Link Partner. 0 = 100BaseT4 not supported by Link Partner.	RO	0
5.8	100Base-TX Full Duplex	1 = 100BaseTX full duplex supported by Link Partner. 0 = 100BaseTX full duplex not supported by Link Partner.	RO	0
5.7	100Base-TX	1 = 100BaseTX supported by Link Partner. 0 = 100BaseTX not supported by Link Partner.	RO	0
5.6	10Base-T Full Duplex	1 = 10Mbps full duplex supported by Link Partner. 0 = 10Mbps full duplex not supported by Link Partner.	RO	0
5.5	10Base-T	1 = 10Mbps supported by Link Partner. 0 = 10Mbps not supported by Link Partner.	RO	0
5.[4:0]	Selector Field	Protocol Selection [00001] = IEEE 802.3.	RO	00001

### Register 6: Auto Negotiation Expansion Register

Reg.bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.4	Parallel Detection Fault	1 = Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can only be cleared by reading this register using the management interface.  0 = No fault detected by parallel detection logic.	RO/LH	0
6.3	Link Partner Next Page Able	1 = Link partner support next page function. 0 = Link partner does not support next page function.	RO	0
6.2	Next Page Able	Next page is supported, i.e., this bit is permanently ties to 1.	RO	1
6.1	Page Received	It is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register.	RO	0
6.0	Link Partner Auto-Negotiation Able	1 = Link partner is Auto-Negotiation capable. 0 = Link partner is not Auto-Negotiation capable.	RO	0





**Register 7: Auto Negotiation Next Page Transmit Register (ANNPTR)**

Reg.bit	Name	Description	Mode	Default
7.15	NP	Next page indication: 1 = Another Next Page desired. 0 = No other Next Page Transfer desired.	RW	0
7.14	Reserved	-	RO	0
7.13	MP	Message page: 1 = Message page. 0 = Un-formatted page.	RW	1
7.12	ACK2	Acknowledge 2 1 = Will comply with message. 0 = Can not comply with message.	RW	0
7.11	TOG_TX	Toggle: 1 = Previous value of transmitted link code word equals to 0. 0 = Previous value of transmitted link code word equals to 1.	RW	0
7.[10:0]	CODE	Message/Un-formatted Code Field.	RW	001



### Register 16: ADMTEK Specific Register

Reg.bit	Name	Description	Mode	Default
16.15	Repeater	1= Repeater mode, full-duplex will be inactive, and CRS only responses to receive activity. SQE test function is also disabled.	RW	Set by RPTR
16.14	INTR_LE VL	INTR pin will be active high if this register bit is set to 1. INTR pin will be active low if this register bit is set to 0.	RW	0
16.[13:12]	Reserved		RW	00
16.11	SQE Test Inhibit	1 = Disable 10BaseT SQE testing. 0 = Enable 10BaseT SQE testing, which will generate a COL pulse following the completion of a packet transmission.	RW	0
16.10	10BaseT Loopback	1 = Enable normal loopback in 10BaseT mode. 0 = Disable normal loopback in 10BaseT mode.	RW	1
16.[9:6]	Reserved	.	RO	0000
16.5	Auto polarity Disable	1 = Disable auto polarity detection / correction. 0 = Enable auto polarity detection / correction.	RW	0
16.4	Reverse Polarity	If Reg. 16.5 is set to 0, and Reverse polarity is detected on the media, this bit will get set to 1. If Reg. 16.5 is set to 1, writing a one to this bit will reverse the polarity of the transmitter. Note: the reverse polarity is detected either through 8 inverted NLP or through a burst of inverted FLP.	RW	0
16.[3:1]	Reserved		RO	000
16.0	Receive Clock Control	Write a one to this bit will shut off RX_CLK when incoming data is not present. RX_CLK will resume active 1 clock cycle prior to RX_DV goes high, and shut off 64 clock cycles after RX_DV goes low. However, in loopback, writing to this bit does not affect RX_CLK. Receive clock will be active all the time.	RW	0

### Register 17: Interrupt Control/Status Register

Reg.bit	Name	Description	Mode	Default
17.15	Jabber IE	Jabber Interrupt Enable.	RW	0
17.14	Rx Er IE	Receive Error Interrupt Enable.	RW	0
17.13	Page_Rx_I E	Page Received Interrupt Enable.	RW	0
17.12	PD_Fault_I E	Parallel Detection Fault Interrupt Enable.	RW	0

17.11	LP_Ack_I E	Link Partner Acknowledge Interrupt Enable.	RW	0
17.10	Link_Not_ OK_IE	Link Status Not OK Interrupt Enable.	RW	0
17.9	R_Fault_IE	Remote Fault Interrupt Enable.	RW	0
17.8	ANeg_Co mp_IE	Auto-Negotiation Complete Interrupt Enable.	RW	0
17.7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17.6	Rx_Er_Int	This bit is set when RX_ER transitions high.	RC	0
17.5	Page_Rx_I nt	This bit is set when a new page is received from link partner during Auto-Neg.	RC	0
17.4	PD_Fault_I nt	This bit is set when parallel detect fault is detected.	RC	0
17.3	LP_Ack_In t	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17.2	Link_Not_ OK Int	This bit is set when link status switches from OK status to Non-OK status (Fail or Ready).	RC	0
17.1	R_Fault_In t	This bit is set when remote fault is detected.	RC	0
17.0	A_Neg_Co mp Int	This bit is set when Auto-Neg is complete.	RC	0

\* See Interrupt Source Table for bit assignments

### Register 18: Diagnostic Register

Reg.bit	Name	Description	Mode	Default
18.[15:12]	Reserved		RO	0000
18.11	DPLX	This bit indicates the result of the Auto-Neg for duplex arbitration.	RO	0
18.10	Speed	This bit indicates the result of the Auto-Neg for data speed arbitration.	RO	0
18.9	RX_PASS	In 10BT mode, this bit indicates that Manchester data has been detected. In 100BT mode, it indicates valid signal has been received but not necessarily locked on to.	RO	0
18.8	RX_LOCK	Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10Base-T or 100Base-TX). This bit is set whenever a cycle-slip occurs, and will remain set until it is read.	RO/SC	0
18.[7:0]	Reserved		RO	0



#### Register 19: Power/Loopback Register

Reg.bit	Name	Description	Mode	Default
19.[14:7]	Reserved		RW	00
19.6	TP125	Transmit transformer ratio selection 1 = 1.25:1 0 = 1:1	RW	0
19.5	Low Power Mode	1 = Enable advanced power saving mode. 0 = disable advanced power saving mode.	RW	1
19.4	Test Loopback	1 = Enable test loopback. Data will be transmitted from MII interface to clock recovery and loopback to MII received data.	RW	0
19.3	Digital loopback	1 = Enable loopback. 0 = Normal operation.	RW	0
19.2	LP_LPBK	1 = Enable link pulse loopback. 0 = Normal operation.	RW	0
19.1	NLP Link Integrity Test	1 = In Auto-Neg test mode, send NLP instead of FLP in order to test NLP receive integrity. 0 = Sending FLP in Auto-Neg test mode.	RW	0
19.0	Reduce Timer	1 = Reduce time constant for Auto-Negotiation timer. 0 = Normal operation.	R	0

#### Register 20: Loopback and Power Management Register

Reg.bit	Name	Description	Mode	Default
20.[15:8]	Reserved		RO	0
20.[7:4]	Cable measurement capability	These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100MHz. The value is a read back from the equalizer, and the measured value is not absolute.	RO	0
20.[3:0]	Reserved		RO	0

### Register 21: Mode Control Register

Reg.bit	Name	Description	Mode	Default
21.15	Reserved		RO	0
21.14	NLP Disable	1 = Force 10B-T link up without checking NLP. 0 = Normal Operation.	RW	0
21.13	Force_link_up	1 = force link up , auto negotiation must be disabled at this time	R/W	0
21.12	Jabber Disable	1 = Disable Jabber function in PHY. 0 = Enable Jabber function in PHY.	RW	0
21.11	10BT_Sel	1 = Enable 7-wire interface for 10Base-T operation. This bit is useful only when the chip is not in PCS bypass mode. 0 = Normal operation.	RW	0
21.[10:9]	Reserved		RO	0
21.8	FEF_Disable	1 = Enable far-end-fault generation and detection function. 0 = Disable far-end-fault.	RW	Set by TECH FX_SEL ANEGA
21.7	Force FEF Transmit	This bit is set to force to transmit Far End Fault (FEF) pattern.	RW	0
21.6	Rx_Er_Cnt_Full	When Receive Error Counter is full, this bit will get set to one.	RO/ RC	0
21.5	Disable Rx_Er_Cnt	1 = Disable Receive Error Counter. 0 = Enable Receive Error Counter.	RW	0
21.4	Dis_WDT	1 = Disable the watchdog timer in the decipher. 0 = Enable watchdog timer.	RW	0
21.3	En_RPBK	1 = Enable remote loopback. 0 = Disable remote loopback.	RW	0
21.2	Dis_Scrm	1 = Enable data scrambling. 0 = Disable data scrambling. When FX mode is selected, this bit will be forced to one.	RW	1
21.[1:0]	Reserved		RO	

### Register 23: PLL Lock Register

Reg.bit	Name	Description	Mode	Default
23.[15:0]	DLOCK drop counter	Count PLL lock drop events.	RW	0000

### Register 24: Receive Error Counter Register

Reg.bit	Name	Description	Mode	Default
24.[15:0]	RX_ER counter	Count receive error events.	RW	0000

● **Electrical Specifications and Timings**

● **Absolute Maximum Ratings**

Supply Voltage (VDD)	-0.3 V to 3.6 V
DC Input Voltage (VIN)	-0.5 V to VDD+0.5V
DC Output Voltage (VOUT)	-0.5 V to VDD+0.5V
<b>Power Consumption</b>	<b>64mA @ Idle state</b>
	<b>120mA @ 10M Full Duplex Mode</b>
	<b>150 mA @ 100M Full Duplex Mode</b>
Storage Temperature	-65 C to 150 C
Ambient Temperature	0 C to 70 C
ESD Rating	2000V

● **Operating Condition**

Symbol	Parameter	Condition	Min	Max	Units
VDD	Supply Voltage		3.0	3.6	V
5VDD	USB Bus Supply Voltage		4.4	5.25	V
I <sub>dd</sub>	Supply Current			150	mA

● **DC Specifications**

**USB Interface DC specification**

Symbol	Parameter	Condition	Min	Max	Units
V <sub>ih</sub>	Input High Voltage		2.0		V
V <sub>il</sub>	Input Low Voltage			0.8	V
I <sub>ih</sub>	Differential Input Sensitivity		0.1		V
V <sub>cm</sub>	Differential Common Mode Range		0.8	2.5	V
V <sub>oh</sub>	Output High Voltage		0.0	0.3	V
V <sub>ol</sub>	Output Low Voltage		2.8	3.6	V
V <sub>crs</sub>	Output Signal Crossover Voltage		0.8	2.5	V

**EEPROM Interface DC specification**

Standard Vcc (4.5V to 5.5V) DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V <sub>ih</sub>	Input High Voltage		2.0	V <sub>cc</sub> +1	V
V <sub>il</sub>	Input Low Voltage		-0.1	0.8	V
I <sub>ih</sub>	Input High Leakage Current	0 < V <sub>in</sub> < V <sub>cc</sub>		1	μA
I <sub>il</sub>	Input Low Leakage Current	0 < V <sub>in</sub> < V <sub>cc</sub>		-1	μA
V <sub>oh</sub>	Output High Voltage	I <sub>oH</sub> = -10 μA	V <sub>cc</sub> -0.2		V
V <sub>ol</sub>	Output Low Voltage	I <sub>oL</sub> = 10 μA		0.2	V
C <sub>in</sub>	Input Pin Capacitance			5	pF

Low Vcc (2.7V to 5.5V) DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V <sub>ih</sub>	Input High Voltage		0.8V <sub>cc</sub>	V <sub>cc</sub> +1	V
V <sub>il</sub>	Input Low Voltage		-0.1	0.15V <sub>cc</sub>	V
I <sub>ih</sub>	Input High Leakage Current	0 < V <sub>in</sub> < V <sub>cc</sub>		1	μA
I <sub>il</sub>	Input High Leakage Current	0 < V <sub>in</sub> < V <sub>cc</sub>		-1	μA
V <sub>oh</sub>	Output High Voltage	I <sub>oH</sub> = -10 μA	0.9V <sub>cc</sub>		V
V <sub>ol</sub>	Output Low Voltage	I <sub>oL</sub> = 10 μA		0.1V <sub>cc</sub>	V
C <sub>in</sub>	Input Pin Capacitance			5	pF

**SRAM Interface DC Specification**

Symbol	Parameter	Condition	Min	Max	Units
V <sub>ih</sub>	Input High Voltage		2.2	V <sub>cc</sub> +0.5	V
V <sub>il</sub>	Input Low Voltage		-0.5	0.8	V
I <sub>ih</sub>	Input High Leakage Current	0 < V <sub>in</sub> < V <sub>cc</sub>		10	μA
I <sub>il</sub>	Input High Leakage	0 < V <sub>in</sub> < V <sub>cc</sub>		-10	μA

# ADMtek Incorporated

## ADM 8511

### Pegasus II USB / Fast Ethernet / HomePNA Controller



	Current				
$V_{oh}$	Output High Voltage	$I_{oH} = -4 \text{ mA}$	2.4		V
$V_{ol}$	Output Low Voltage	$I_{oL} = 8 \text{ mA}$		0.4	V

#### HomePNA Interface DC Specification

Symbol	Parameter	Condition	Min	Max	Units
$V_{ih}$	Input High Voltage		2.0		V
$V_{il}$	Input Low Voltage			0.8	V
$I_{ih}$	Input High Leakage Current	$0 < V_{in} < V_{cc}$		10	$\mu\text{A}$
$I_{il}$	Input Low Leakage Current	$0 < V_{in} < V_{cc}$		-10	$\mu\text{A}$
$V_{oh}$	Output High Voltage	$I_{oH} = -4 \text{ mA}$	$V_{cc} - 0.5$		V
$V_{ol}$	Output Low Voltage	$I_{oL} = 4 \text{ mA}$		0.4	V

#### GPIO Interface DC Specification

Symbol	Parameter	Condition	Min	Max	Units
$V_{ih}$	Input High Voltage		2.0		V
$V_{il}$	Input Low Voltage			0.8	V
$I_{ih}$	Input High Leakage Current	$0 < V_{in} < V_{cc}$		10	$\mu\text{A}$
$I_{il}$	Input Low Leakage Current	$0 < V_{in} < V_{cc}$		-10	$\mu\text{A}$
$V_{oh}$	Output High Voltage	$I_{oH} = -4 \text{ mA}$	2.4		V
$V_{ol}$	Output Low Voltage	$I_{oL} = 4 \text{ mA}$		0.4	V

## ● Timings

### Reset Timing

ADM8511 can be reset either by hardware, software or USB reset.

1. A hardware reset is accomplished by asserting the RST# pin after power up the device. It should have a duration of at least 100 ms to ensure the external 48MHz crystal is in stable and correct frequency. All registers will be reset to default values.
2. A software reset is accomplished by setting the reset bit (bit 4) of the Ethernet Control Register (address 01h). This software reset will reset all registers to default values.
3. When ADM8511 sees an SE0 on USB bus for more than 2.5 $\mu\text{s}$ . This USB reset will reset



### USB Interface Timing

Symbol	Parameter	Condition	Min	Max	Units
$T_{fr}$	Rise Time		4	20	ns
$T_{ff}$	Fall Time		4	20	ns
$T_{fftm}$	Differential Rise and Fall Time Matching	$T_{FR} / T_{FF}$	90	111.11	%
$T_{fdrate}$	Full-speed Data Rate		11.9700	12.0300	Mb/s
$T_{feopt}$	Source SE0 interval of EOP		160	175	ns
$T_{fst}$	Width of SE0 interval during differential transition			14	ns

### EEPROM Interface Timing

Symbol	Parameter	Min	Max	Units
$t_{EESK}$	<b>EESK</b> Clock Frequency	0	1	MHz
$T_{EECSS}$	<b>EECS</b> Setup Time to <b>EESK</b>	0.2		$\mu$ s
$T_{EECSH}$	<b>EECS</b> Hold Time from <b>EESK</b>	0		ns
$T_{EEDOH}$	<b>EEDO</b> Hold Time from <b>EESK</b>	70		ns
$T_{EEDOP}$	<b>EEDO</b> Output Delay to "1" or "0"		2	$\mu$ s
$t_{EEDIS}$	<b>EEDI</b> Setup Time to <b>EESK</b>	0.4		$\mu$ s
$t_{EEDIH}$	<b>EEDI</b> Hold Time from <b>EESK</b>	0.4		$\mu$ s

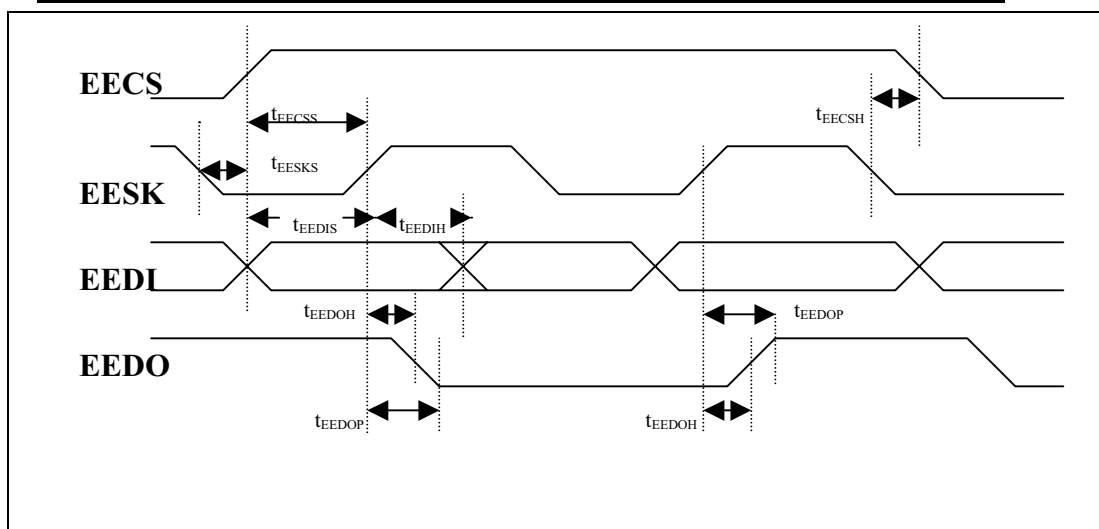


Fig. 1 EEPROM Interface Timings

● SRAM Interface Timing

Access time less than 15ns is supported.

Read cycle switching characteristics of access time 15ns.

Symbol	Parameter	Min	Max	Units
$t_{rc}$	Read Cycle Time	15		ns
$t_{aa}$	Address Access Time		15	ns
$t_{oha}$	Output Hold Time	2		ns
$t_{ace}$	CE Access Time		15	ns
$t_{doe}$	OE Access Time		7	ns

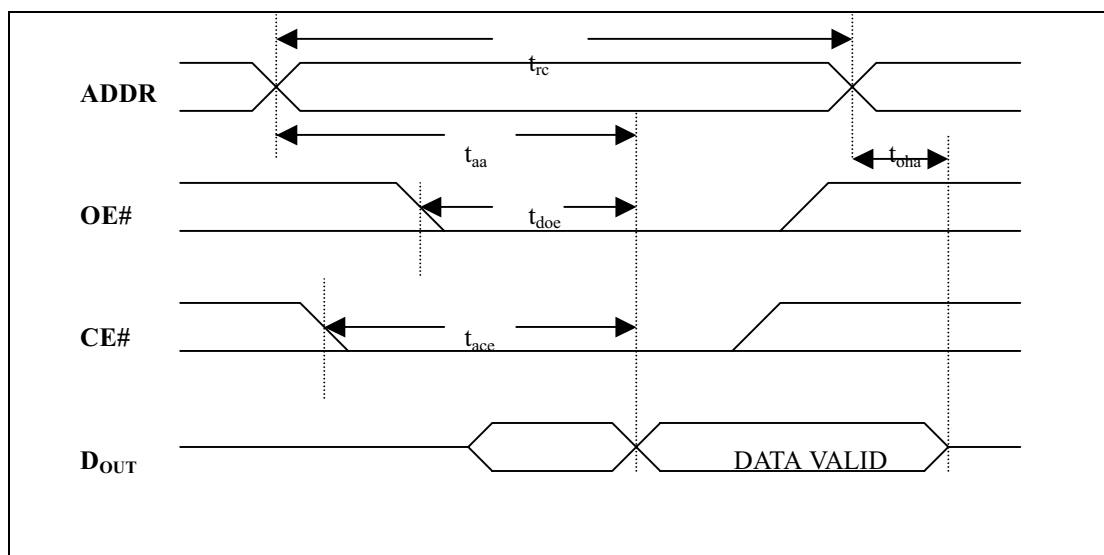
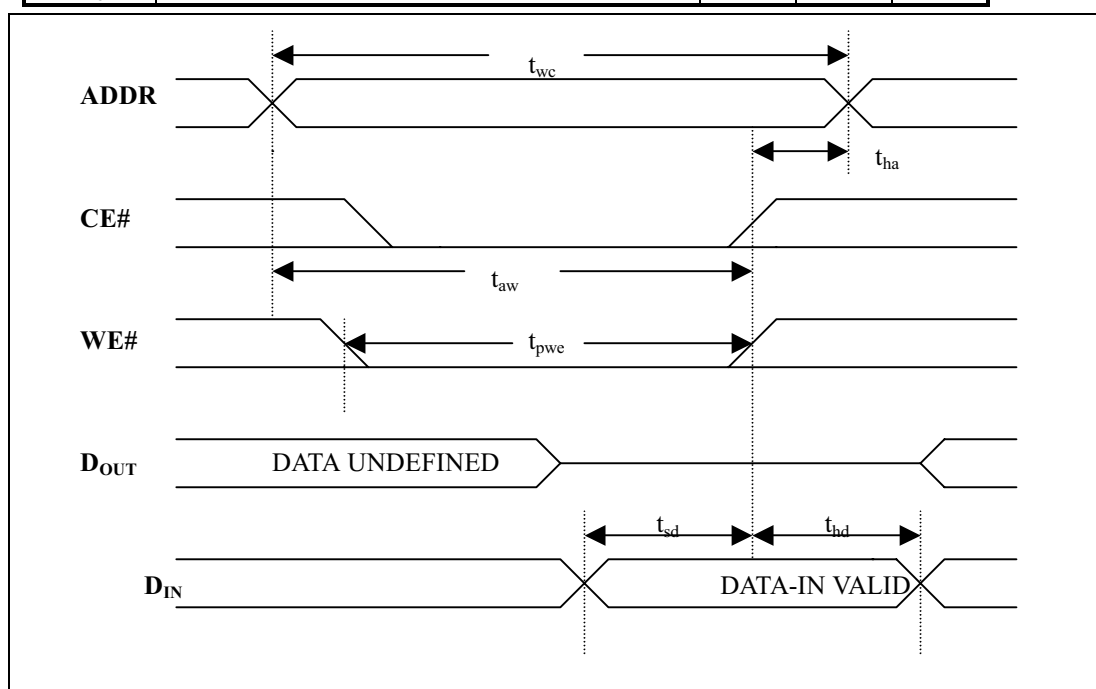


Fig. 2 SRAM Interface Read Cycle Timings

Write cycle switching characteristics of access time 15ns.

Symbol	Parameter	Min	Max	Units
$t_{wc}$	Write Cycle Time	15		ns
$t_{aw}$	Address Setup Time to Write End	10		ns
$t_{ha}$	Address Hold Time from Write End	0		ns
$t_{pwe}$	WE Pulse Width	10		ns
$t_{sd}$	Data Setup Time to Write End	9		ns
$t_{hd}$	Data Hold Time from Write End	0		ns



**Fig. 3 SRAM Interface Write Cycle Timings**

● **HomePNA Interface Timing**

Symbol	Parameter	Min	Max	Units
1	HPN_TXCLK during MAC preamble and delimiter	100e-9	100e-6	Sec
	HPN_TXCLK during Ethernet packet	100e-9	10e-6	Sec
	HPN_RXCLK during MAC preamble and delimiter	100e-9	100e-6	Sec
	HPN_RXCLK during Ethernet packet	100e-9	10e-6	Sec
	HPN_TXCLK and HPN_RXCLK during 96-bit inter-frame gap	233.33 4	233.33 4	ns
	HPN_TXCLK and HPN_RXCLK during idle	583.33 5	583.33 5	ns

● MII Interface Timing

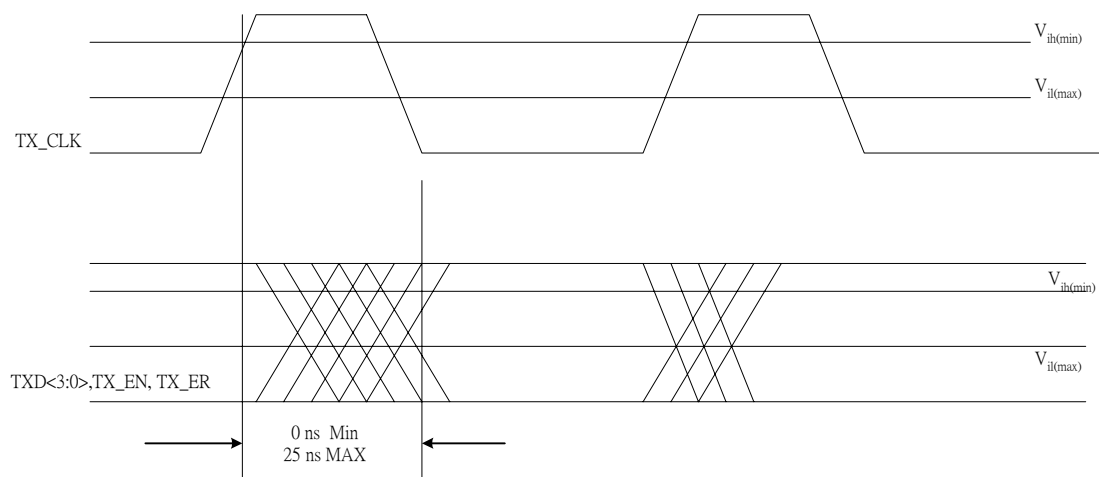


Fig. 4 Transmit signal timing relationships at the MII

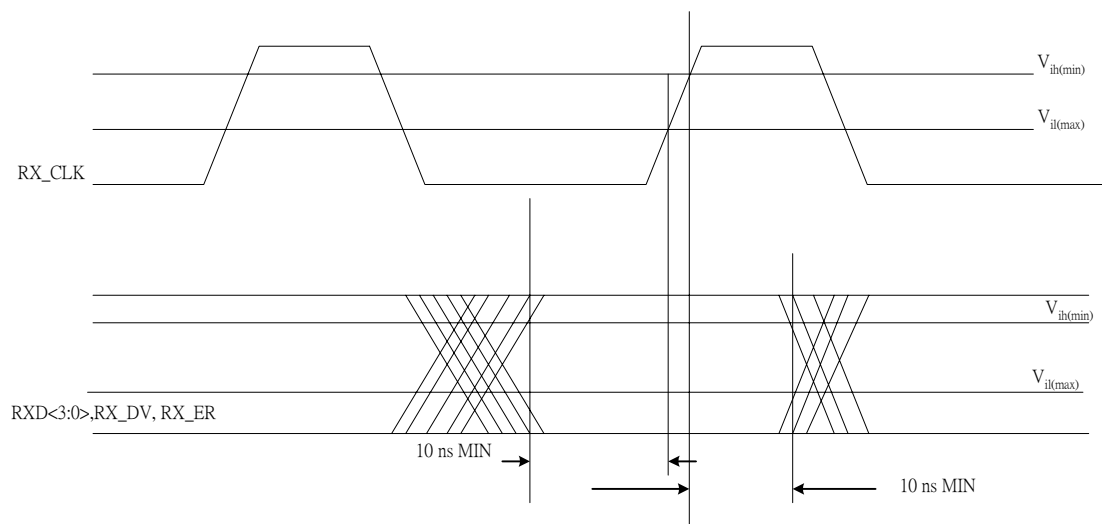
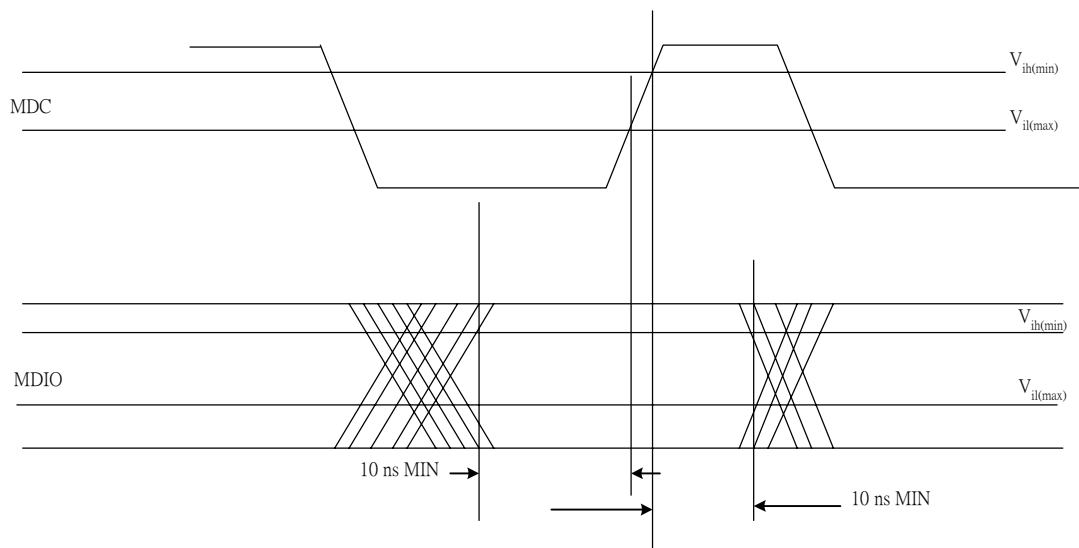
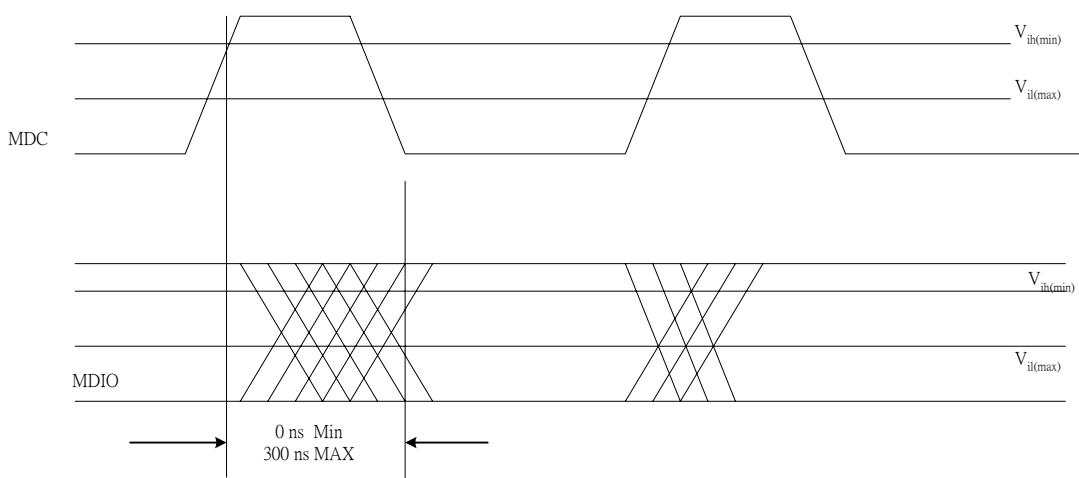


Fig. 5 Receive signal timing relations at the MII



**Fig. 6 MDIO sourced by STA**



**Fig. 7 MDIO sourced by PHY**

12. Package

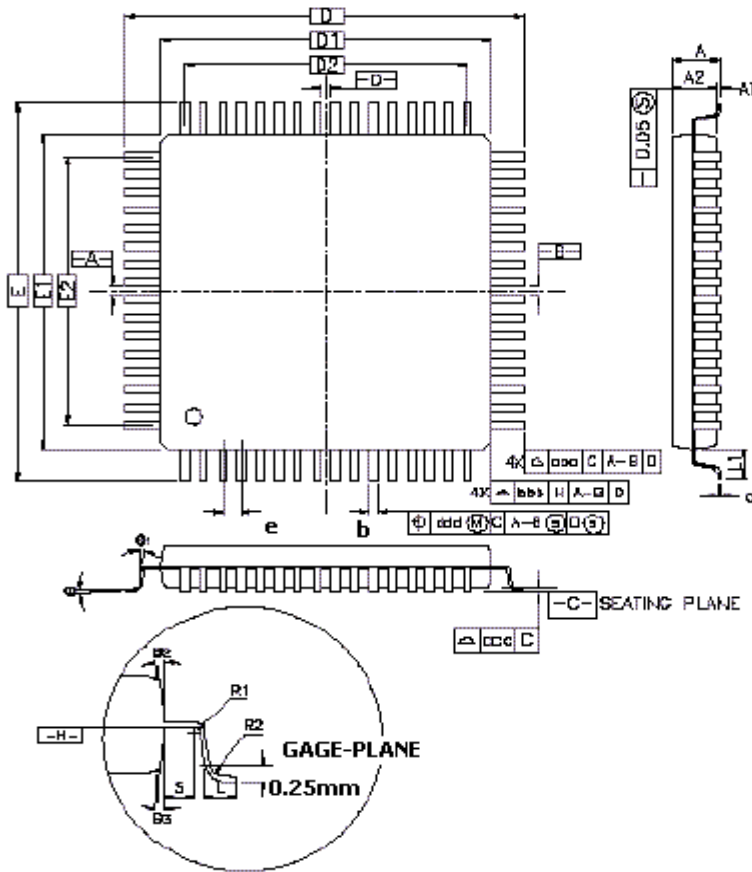


Fig. 8 Package outline of ADM8511

**Dimensions for 100 pin LQFP Package**

Symbol	Millimeter (mm)			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-----	-----	1.60	-----	-----	0.063
A <sub>1</sub>	0.05	-----	0.15	0.002	-----	0.006
A <sub>2</sub>	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D <sub>1</sub>	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E <sub>1</sub>	14.00 BSC.			0.551 BSC.		
R <sub>2</sub>	0.08	-----	0.20	0.003	-----	0.008
R <sub>1</sub>	0.08	-----	-----	0.003	-----	-----
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ <sub>1</sub>	0°	-----	-----	0°	-----	-----
Θ <sub>2</sub>	11°	12°	13°	11°	12°	13°
Θ <sub>3</sub>	11°	12°	13°	11°	12°	13°
c	0.09	-----	0.20	0.004	-----	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L <sub>1</sub>	1.00 Ref			0.039 Ref		
S	0.20	-----	-----	0.008	-----	-----
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC,			0.020 BSC.		
D <sub>2</sub>	12.00			0.472		
E <sub>2</sub>	12.00			0.472		
Tolerance of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

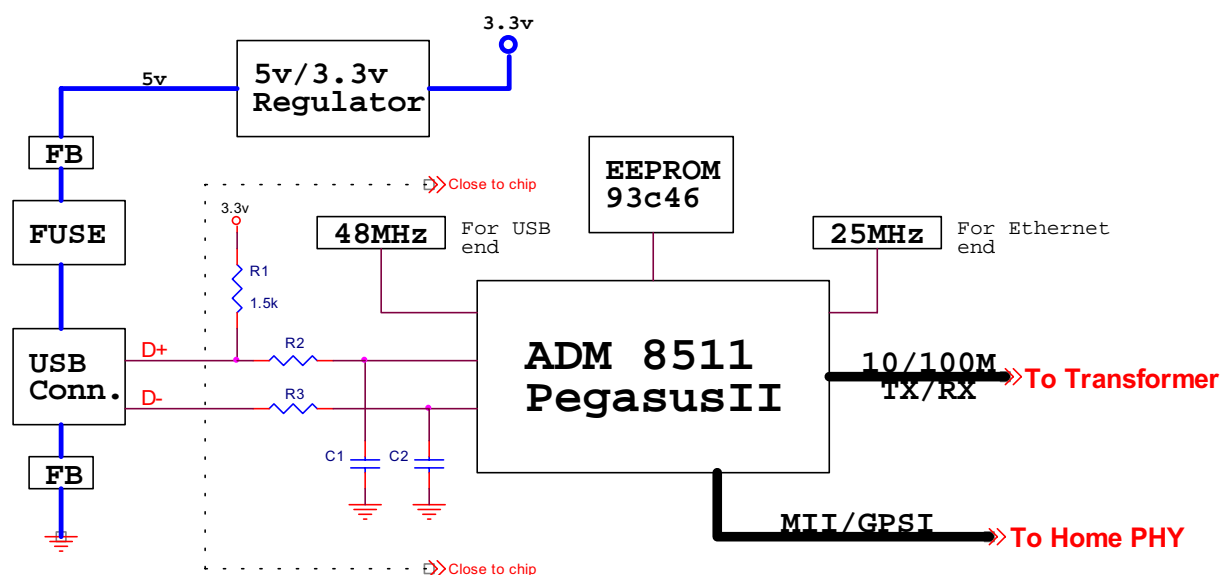
**Notes :**

- Dimensions D<sub>1</sub> and E<sub>1</sub> do not include mold protrusion. Allowable protrusion is 0.25mm per. Side D<sub>1</sub> and E<sub>1</sub> are Maximum plastic body size dimensions including mold mismatch.
- Dimension b does not include dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4 mm and 0.5mm pitch packages.

## APPENDIX 1    Layout Guide

### 1.Placement:

- (1) On USB side, Place PegasusII and USB connector as close as possible.
- (2) On Ethernet side, place PegasusII ,transformer and RJ45 as close as possible .
- (3) The crystal or OSC device should be close to PegasusII and away from the following items:
  - Any analog signal
  - PCB edge
  - Any other high frequency components and their associated traces.
- (4) Place the filtering capacitor as close as possible at the power pin of ADM 8511 (Pegasus II) and its trace is short and wide.

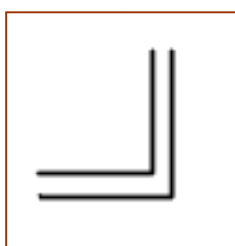


### 2.Trace routing

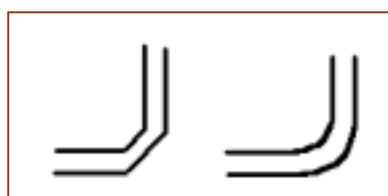
- (1) Keep USB differential pair data signal D+ and D-:
  - Trace width should be as wide as possible.
  - Make D+ and D- traces route at the same signal plane and doesn't pass through other plane .
  - Inhibit crossover on D+ and D-
  - The termination resistance (R2,R3) and decoupling capacitors (C1,C2) should be close to ADM8511.
  - D+ and D- Signal trace length should be equal and as short as possible.
- (2) Arrangement Tx and Rx trace



- Tx+/- and Rx+/- trace avoid right angle and round angle >90 degree; suggested.



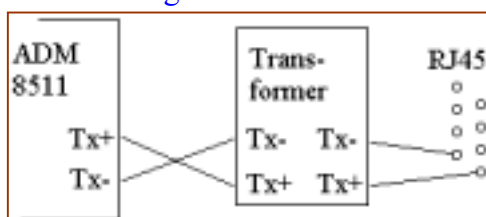
Bad



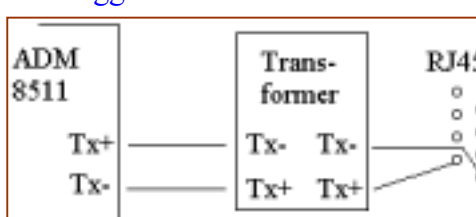
Good

- Trace width must be wide and should be wider than 8 mils.
  - Signal trace length between Tx+/- differential pairs should be cross and have equal length .The total length should be no longer than 2 cm. The same requirement also apply to Rx+/-.
  - Make Tx and Rx trace route at the same signal plane and doesn't pass through other plane.
  - Every differential pairs as cross as possible, but no less than 8 mils and space should be almost equal .
  - Keep space large between Tx and Rx differential pairs, even separated ground planes underneath Tx and Rx signal pairs.
  - Away from clock and power traces.
  - If Tx routed trace must cross, the trace can be swapped between chip and transformer, and transformer to RJ45 ,too.

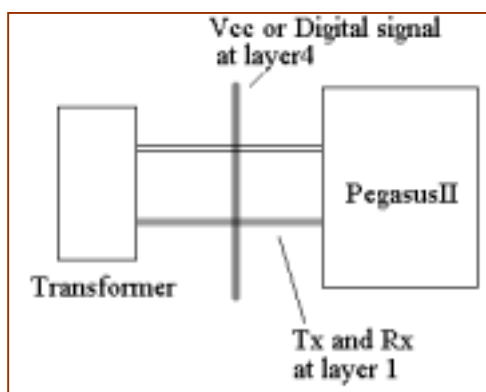
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Suggest

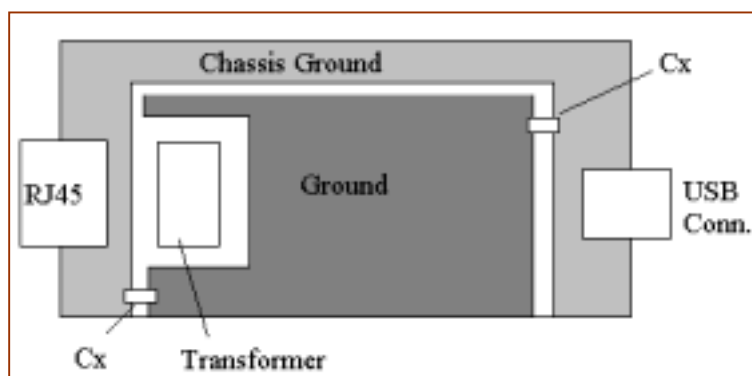


- (3) Digital signal should be away from analog signal and power traces .If this can't be avoid , analog and Vcc should cross over 90 degree at other plane.
- (4)Vcc trace should short and prefer to route in [this plane format](#), special for GND.

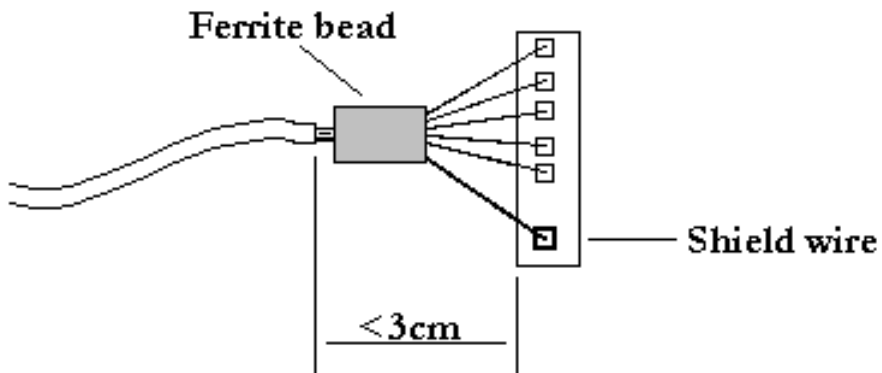


### 3. Power and Ground

- (1) Every power pin should have 0.1uF SMD capacitors placed with it. To be effective, the capacitors should be placed as close as possible at the pin.
- (2) The chassis ground plane connected to the USB B type and network connector chassis should be isolated from the signal plane with 0.1uF capacitors or bead to prevent any radiation from leaking and resulting in FCC failure.
- (3) Right angle is recommend when partition Vcc as well as GND planes.
- (4) Avoid power and ground planes placing directly under the transformer. [See the Figure as below.](#)



- (5) If you use a permanently attached cable (plus the shield wire), it may require additional filtering for FCC test pass, and the length of unshielded cable should be limited to 3cm or less.





## APPENDIX 2 EEPROM Interface & Example

### General EEPROM Format Description

If the EEPROM contents from offset 0 to offset 5 is “FF\_FF\_FF\_FF\_FF\_FF”, it means the EEPROM isn’t programmed correctly, The default values for every field are used instead of loading from EEPROM.

Offset(byte)	Field	Description
00	node_id0	The 1st byte of Ethernet node ID.
01	node_id1	The 2nd byte of Ethernet node ID.
02	node_id2	The 3rd byte of Ethernet node ID.
03	node_id3	The 4th byte of Ethernet node ID.
04	node_id4	The 5th byte of Ethernet node ID.
05	node_id5	The 6th byte of Ethernet node ID.
06-07	reserved	
08	max_pwr	The maximum USB power consumption.
09	ep3_interval	The polling interval for endpoint 3. If this value is 0, EP3 is disabled.
0A[0]	iso_enable	Isochronous endpoint enable
0A[1]	USB transceiver Test_mode	0: select external USB transceiver. 1: select internal USB transceiver.
0A[4:2]	MII Test_mode	000b: tri-state MII pins 001b: enable MAC’s MII signals to external interface 010b: enable PHY’s MII signals to external interface 011b: monitor MII mode
0B	reserved	
0C	languageid_lo	The low byte of language ID.
0D	languageid_hi	The high byte of language ID.
0E-0F	reserved	
10	manuid_lo	The low byte of manufacture ID.
11	manuid_hi	The high byte of manufacture ID.
12	proid_lo	The low byte of product ID.
13	proid_hi	The high byte of product ID.
14	manu_str_len	The length for manufacture string.
15	manu_str_offset	The word offset address of manufacture string.
16	pro_str_len	The length for product string.
17	pro_str_offset	The word offset address of product string.
18	seri_str_len	The length for serial number string.
19	seri_str_offset	The word offset address of serial number string.

### Example

<u>offset(byte)</u>	<u>value</u>
0000h:	00, 00, E8, 10, 46, 02, 00, 00,
0008h:	50, 01, 02, 00, 09, 04, 00, 00,
0010h:	A6, 07, 86, 19, 0E, 10, 1E, 18,

# ADMtek Incorporated

## ADM 8511

Pegasus II

USB / Fast Ethernet / HomePNA Controller



0018h: 0A, 28, 00, 00, 00, 00, 00, 00,  
0020h: 0E, 03, 41, 00, 44, 00, 4D, 00,  
0028h: 74, 00, 65, 00, 6B, 00, 00, 00,  
0030h: 1E, 03, 55, 00, 53, 00, 42, 00,  
0038h: 20, 00, 31, 00, 30, 00, 2F, 00,  
0040h: 31, 00, 30, 00, 30, 00, 20, 00,  
0048h: 4D, 00, 41, 00, 43, 00, 00, 00,  
0050h: 0A, 03, 30, 00, 30, 00, 30, 00,  
0058h: 31, 00, 00, 00, 00, 00, 00, 00,  
0060h: 00, 00, 00, 00, 00, 00, 00, 00,  
0068h: 00, 00, 00, 00, 00, 00, 00, 00,  
0070h: 00, 00, 00, 00, 00, 00, 00, 00,  
0078h: 00, 00, 00, 00, 00, 00, 00, 00

Offset(byte)	Value	Description
00-05	00 00 E8 10 46 02	NIC node ID
08	50	maximum power 160mA
09	01	interrupt endpoint 3 polling interval 1ms
0A	02	isochronous endpoint disable, select internal USB transceiver Use internal Ethernet PHY
0C-0D	0904	Language ID 0409
10-11	A607	manufacture ID 07A6
12-13	8619	product ID 1986
14	0E	manufacture string length 0E bytes
15	10	manufacture string starts from word offset 10h, thus byte offset 20h.
16	1E	product string length 1E bytes
17	18	product string starts from word offset 18h, thus byte offset 30h.
18	0A	serial number string length 0A bytes
19	28	serial number string starts from word offset 28h, thus byte offset 50h.
20-2E	0E 03 41 00 44 00 4D 00 74 00 65 00 6B 00	0E:descriptor size 14 bytes 03: string descriptor 41.....: UNICODE encoded string
30-4E	1E 03 55 00 53 00 42 00 20 00.....	1E:descriptor size 30 bytes 03: string descriptor 55.....: UNICODE encoded string
50-5A	0A 03 30 00 30 00 30 00 31 00	0A: descriptor size 10 bytes 03: string descriptor 30.....: UNICODE encoded string

## APPENDIX 3 USB Device Operation

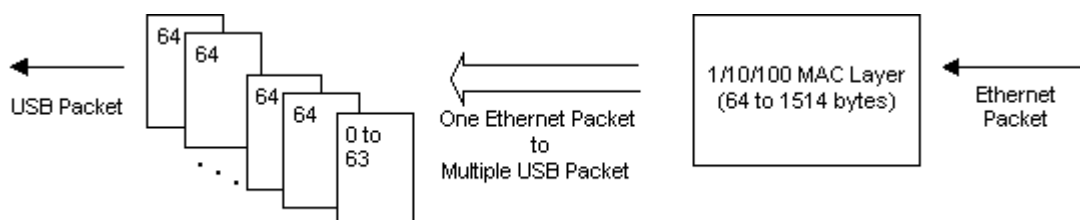
### Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal registers setting are also via this endpoint. The response to each command is described in section 7.

### Endpoint 1 bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 64-byte USB packets on USB. The end of the Ethernet packet is indicated by less than 64-byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint if RX FIFO is either full or any packet is inside, the data in RX FIFO is returned in USB data stage. If ACK is received from USB host, data in RX FIFO is flushed. If no response or NAK is received from USB host, the content in RX FIFO will be re-transmitted. If RX FIFO isn't ready for transmission, NAK is returned to USB host.



The received status is reported as follows

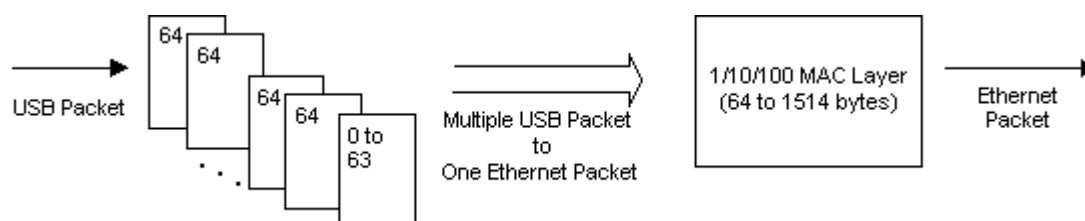
Offset	Bit	Field	Description
Offset0	7-0	rx_bytecnt_lo	The received byte count[7:0].
Offset1	3-0	rx_bytecnt_hi	The received byte count[11:8].
	7-4	Reserved	
Offset2	0	Multicast_frame	Indicate receive a multicast frame.
	1	Long_pkt	Indicate received packet length > 1518 bytes.
	2	Runt_pkt	Indicate received packet length < 64 bytes.
	3	crc_err	Indicate CRC check error.
	4	Dribble_bit	Indicate packet length is not integer multiple of 8-bit.
	7-5	Reserved	
Offset3	7-0	Reserved	

### Endpoint 2 bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated as multiple 64-byte USB packets on USB. The first two bytes in every first concatenated USB packet indicate the total length of the Ethernet packet. The end of the Ethernet packet is indicated with less than 64-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When access to this endpoint, data in USB data stage is transfer to TX FIFO when TX FIFO is free and ACK is returned. If TX FIFO isn't free, NAK is returned.

Field	1st byte in 1st USB packet	2nd byte in 1st USB packet	The following packets
Content	len[7:0]: Low byte Ethernet packet length	{reserved[4:0], len[10:8]}	Ethernet packet



### Endpoint 3 interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When access to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains

Offset0	Offset1	Offset2	Offset3	Offset4
tx_status(Reg2Bh)	tx_status(Reg2Ch)	rx_status(Reg2Dh)	rx_lostpkt(Reg2Eh)	rx_lostpkt(Reg2Fh)

Offset5	Offset6-7(2B)
Wakeup_status(Reg7Ah)	0



## APPENDIX 4 USB Command

### Get\_Register (Vendor Specific) Single/Burst read

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
C0	F0	0	{RegIndex[0:7], 00}	length

■ Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}

The returned total number of registers depends on the length field.

### Set\_Register (Vendor Specific) Single write

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	{value[0:7],mask[0:7]}	{RegIndex[0:7], 00}	1

### Set\_Register(Vendor Specific) Burst write

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	F1	0	{RegIndex[0:7], 00}	length

■ Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}	{RegIndex+3}

Ex. Write 44 to RegIndex=05h, the transfer will be

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	FE	4400	0500	0100

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported

=> DataStage for 8-byte OUT transfer appears

Ex. Burst write 20 registers from RegIndex=07h and data from 01<sub>d</sub> to 20<sub>d</sub>

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
40	FE	0000	0700	1400



# ADMtek Incorporated

## ADM 8511

Pegasus II

USB / Fast Ethernet / HomePNA Controller



### ■ Data Stage

#### ➤ 1st OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
01	02	03	04	05	06	07	08

#### ➤ 2nd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
09	0A	0B	0C	0D	0E	0F	10

#### ➤ 3rd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)
11	12	13

## Get\_Status(Device)

### ■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	0	0	0	2

### ■ Data Stage

D[15:2]	D[1]: Remote Wakeup	D[0]: Self Powered
0	register of remote_wakeup	1

## Get\_Status(Interface)

### ■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
81	0	0	0	2

### ■ Data Stage

D[15:0]
0

## Get\_Status(EP0)

### ■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0080 or 0000	2

### ■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep0_halt

### Get\_Status(EP1) bulk IN

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0081	2

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep1_halt

### Get\_Status(EP2) bulk OUT

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0002	2

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep2_halt

### Get\_Status(EP3) interrupt IN

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
82	0	0	0083	2

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep3_halt

### Get\_Descriptor(Device) total 18-byte

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	6	0001	0	length

■ Data Stage: wLength field specifies the total byte count to return

Offset0	Offset1(type)	Offset2(USB release no.)	Offset4(Class code)	Offset5(Sub Class Code)	Offset6(Protocol)	Offset7(EP0 MaxPktSize)	Offset8 (vendor ID)
12(1B)	01(1B)	0110(2B)	00(1B)	00(1B)	00(1B)	8(1B)	(2B)

Offset10 (productID)	Offset12(releaseID)	Offset14 (manufacture)	Offset15 (Product)	Offset16(serial no.)	Offset17(no. of config)
(2B)	0001(2B)	01(1B)	02(1B)	03(1B)	01(1B)



#### Get\_Descriptor(Configuration) total 39-byte

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	6	0002	0	length

■ Data Stage

➤ Configuration Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (TotalLength)	Offset4 (NumInterface)	Offset5 (ConfigValue)	Offset6 (StringIndex)	Offset7 (Attribute)	Offset8 (MaxPower)
09(1B)	02(1B)	0027(2B)	01(1B)	00(1B)	00(1B)	E0(1B)	max_pwr(1B)

➤ Interface 0 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (InterfaceNum)	Offset3 (AltInterface)	Offset4 (NumEP)	Offset5 (IntfClass)	Offset6 (IntfSubClass)	Offset7 (IntfProtocol)	Offset8 (StringIndex)
09(1B)	04(1B)	00(1B)	00(1B)	04(1B)	xx(1B)	E0(1B)	xx(1B)	00(1B)

➤ EP1 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	81(1B)	02(1B) bulk	0064(2B)	00(1B)

➤ EP2 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	02(1B)	02(1B) bulk	0064(2B)	00(1B)

➤ EP3 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4 (MaxPktSize)	Offset6 (Interval)
07(1B)	05(1B)	83(1B)	03(1B) interrupt	0008(2B)	ep3_interval(1B)

#### Get\_Descriptor(String) Index0, LanguageID Code

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0003	0000	length

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	Offset2 (LanguageID)
04(1B)	03(1B)	0904(2B)



#### Get\_Descriptor(String) Index1, manufacture

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0103	0904	length

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

#### Get\_Descriptor(String) Index2, product

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0203	0904	length

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

#### Get\_Descriptor(String) Index3, serial no.

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	06	0303	0904	length

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	
Length(1B)	03(1B)	String

#### Get\_Configuration

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
80	08	0	0	0001

■ Data Stage

Offset0 (ConfigValue)(1B)



#### Get\_Interface

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
81	10	0	0	0001

■ Data Stage

Offset0 (AltIntf)(1B)
00

#### Set\_Address

#### Set\_Configuration

#### Set\_Interface

#### Clear\_Feature(Device) Remote Wakeup

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
00	01	0100	0	0

#### Set\_feature(Device) Remote Wakeup

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
00	03	0100	0	0

#### Clear\_Feature(EP0,1,2,3) Halt

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
02	03	0000	{00, EP no}	0

#### Set\_Feature(EP0,1,2,3) Halt

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength(2B)
02	03	0000	{00, EP no}	0

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**APPENDIX 5 Design Notes for Ethernet & HomePNA Application**

**1.48MHz Crystal**

It was a 3 times frequency circuit. So it uses a 16MHz crystal in the demo (reference) schematic. However, 48MHz crystal is also valid and associates with tow ceramic capacitor.

**2.SRAM**

All of the SRAM pin can be NC (No Connection).

**3.RST# and POREN\_N**

a.Internal Power On Reset in ethernet only or combo (Ethernet & HPNA) solution:

The ADM8511 provides internal power reset. In ethernet only or combo sloution,you can let RST# and POREN\_N pin NC.

b.External reset in external PHY only solution.(e.g. Home PNA only)

POREN\_N need pull to high and RST# need a reset cell (e.g. RC circuit) to provide a low pulse to reset ADM8511. It should have a duration of at least 50 ms (the best is more than 100ms) to ensure that the external 48MHz crystal is in stable and correct frequency. All registers will be reset to default values. In our suggestion design, the reset network provides more than 80ms low pulse.

**4.XLNKSTS:**

a.Ethernet only solution:

This pin need strapping to low directly.

c.Combo or External PHY only solution:

reports link status information to system and level change trigger.

**5.LED**

all of the LED pin are active Low and only display internal PHY status.

**6.Ethernet pin (LED,XTLP/N,TXOP/N,RXIP/N,RIBB,TST0...3)**

In External PHY solution ,All can be NC.

**7.MII interface signal pins**

a.In ethernet only solution:

All of the MII pin can be NC.

b.In combo or external PHY only solution:

- i. MDIO rquires external 1.5k pull-up resistor.
- ii. TXEN requires external 4.7k pull-down resistor.

If the external PHY did not provide **RXER**, this pin needs strapping to low directly.